2017 International Symposium on

VLSI Technology, Systems and Applications

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III-V Channel Transistors

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MIT

Acknowledgements:

- Students and collaborators: D. Antoniadis, J. Lin, W. Lu, A. Vardi, X. Zhao
- Sponsors: Applied Materials, DTRA, KIST, Lam Research, Northrop Grumman, NSF, Samsung
- Labs at MIT: MTL, EBL

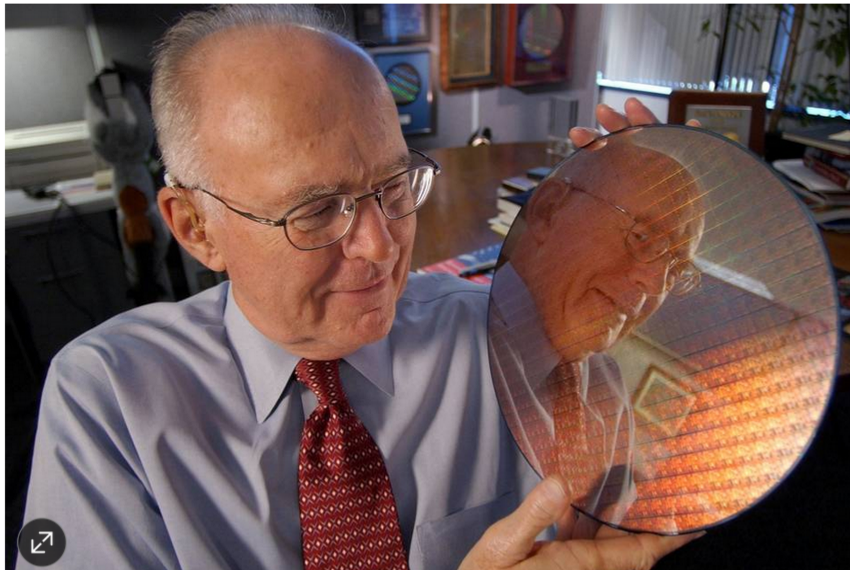
24 April 2017

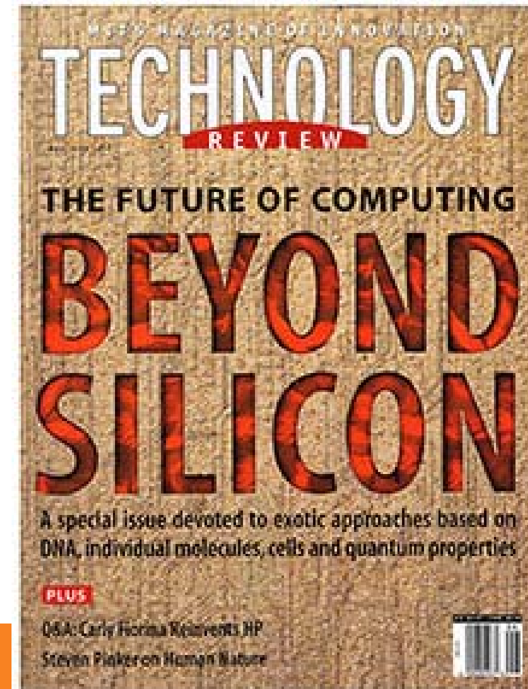
Moore's Law at 50: the end in sight?

THE WALL STREET JOURNAL.

Moore's Law Is Showing Its Age

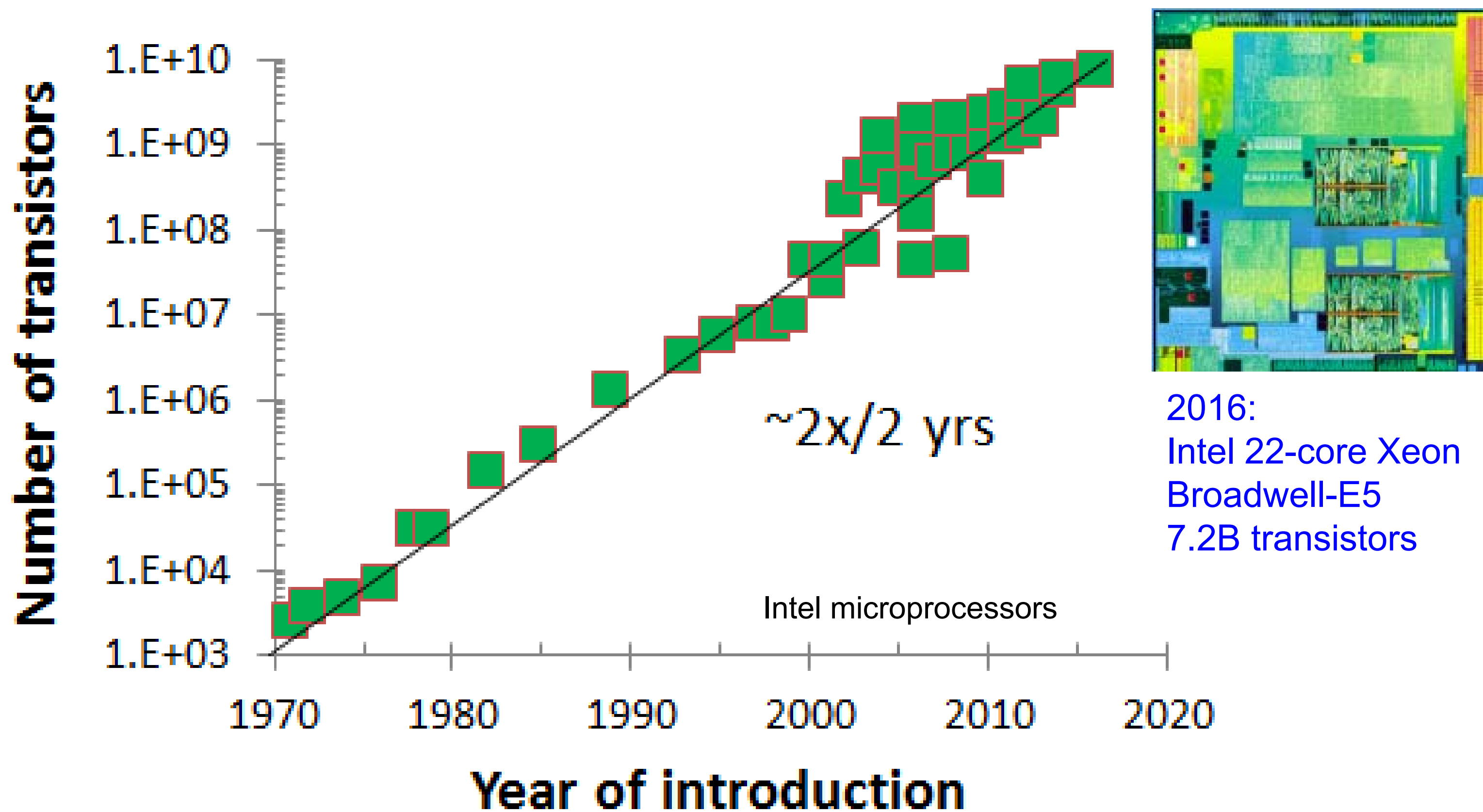
The prediction about squeezing transistors onto silicon has been revised again.





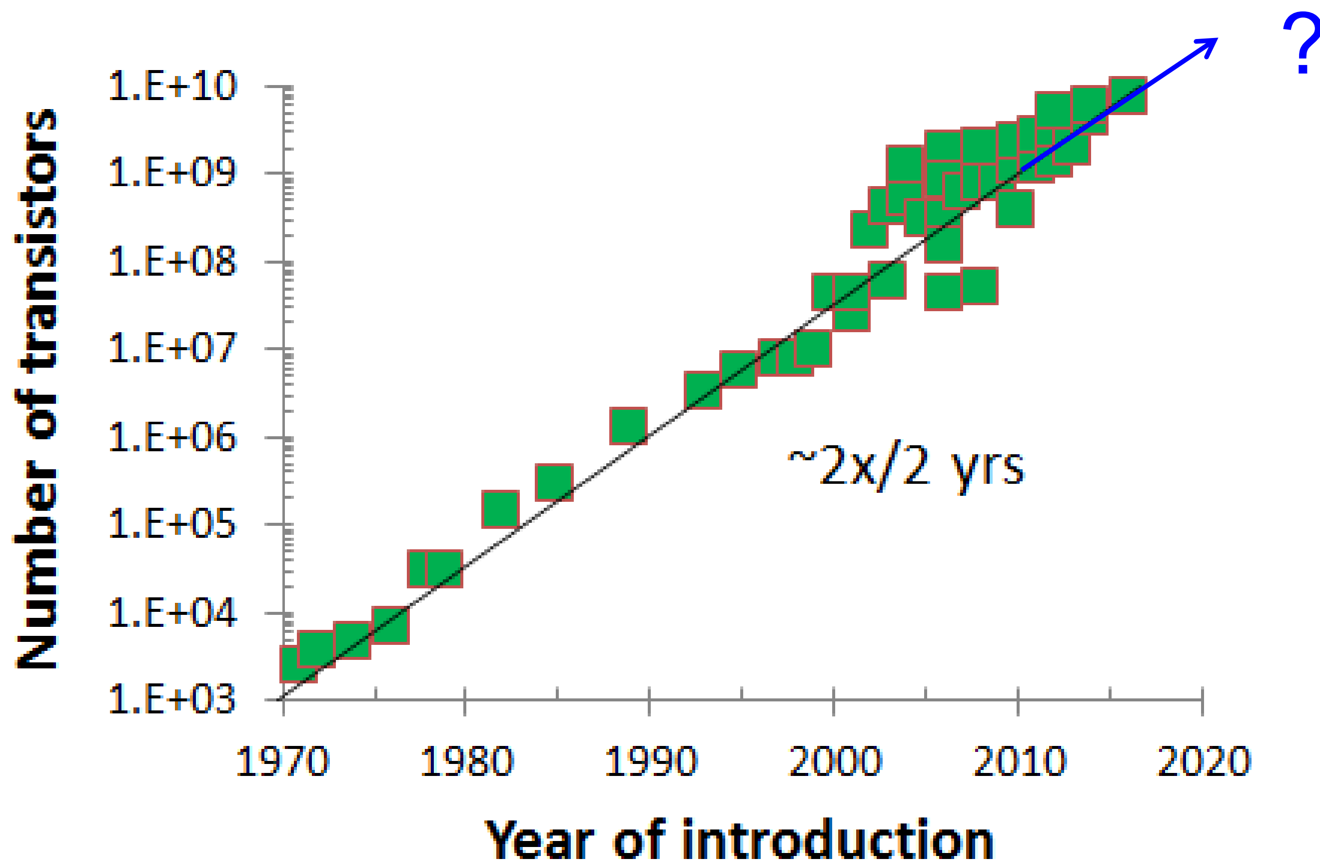
Moore’s Law

Moore’s Law = exponential increase in transistor density



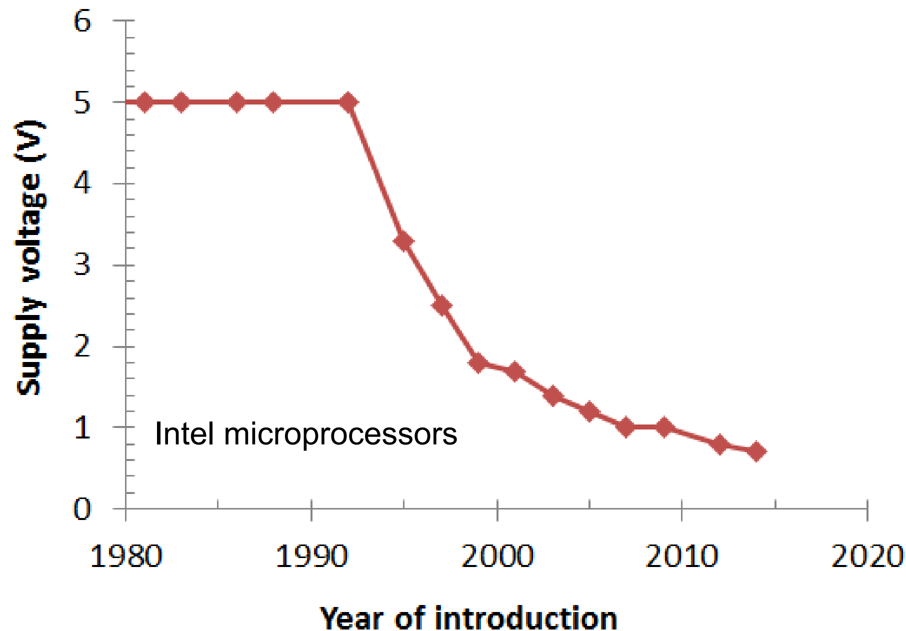
Moore's Law

How far can Si support Moore's Law?

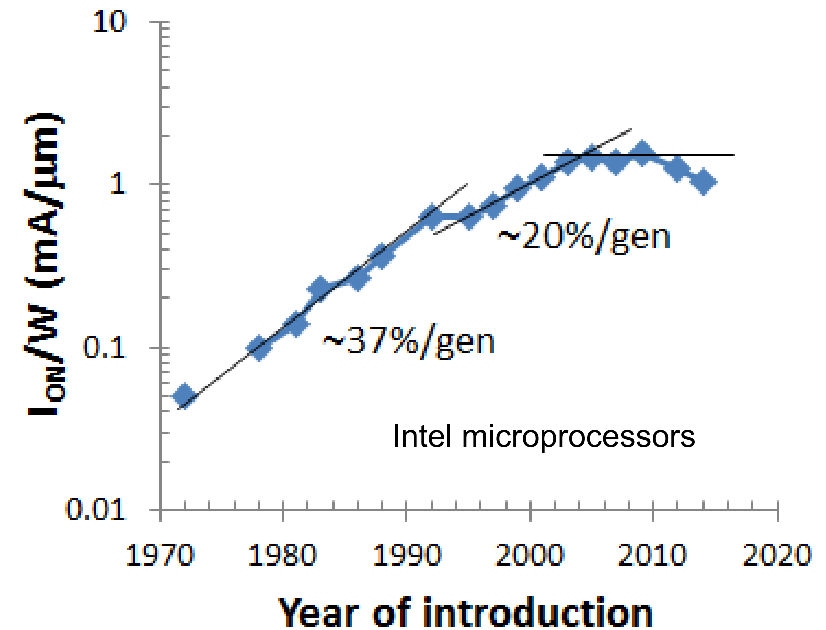


Transistor scaling → Voltage scaling → Performance suffers

Supply voltage:



Transistor current density:

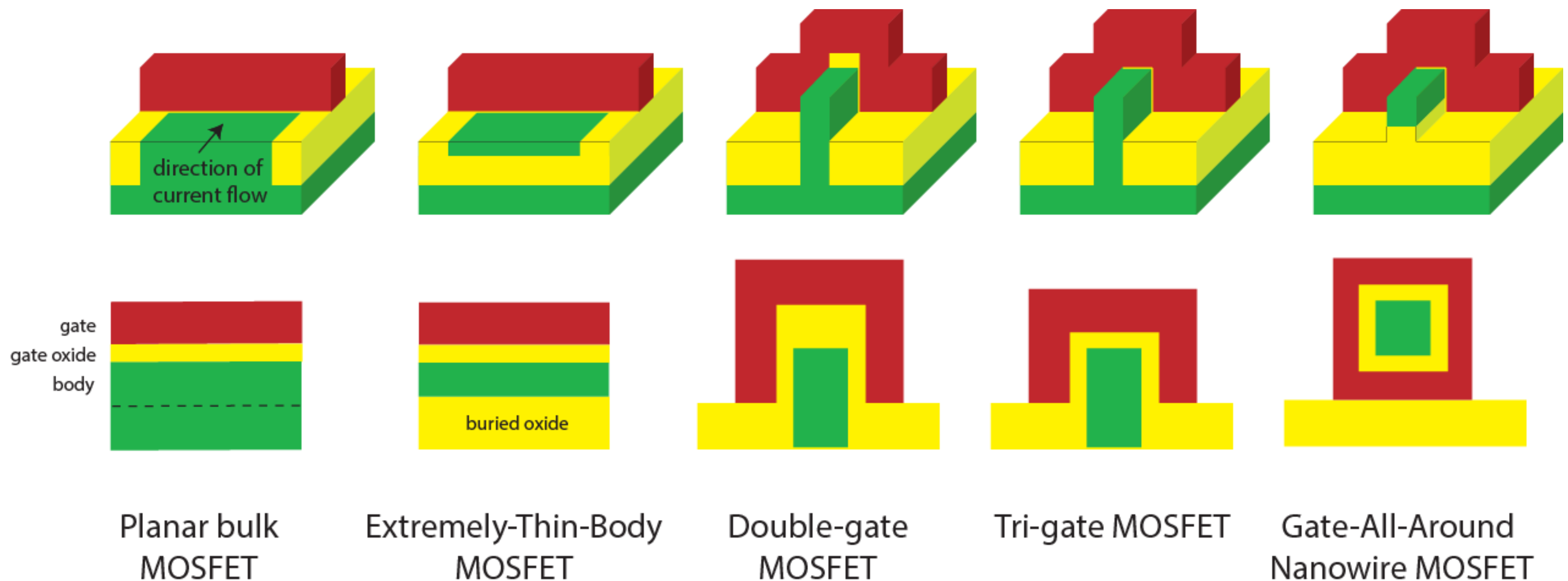


Goals:

- Reduced footprint with moderate short-channel effects
- High performance at low voltage

Moore's Law: it's all about MOSFET scaling

1. New device structures with improved scalability:

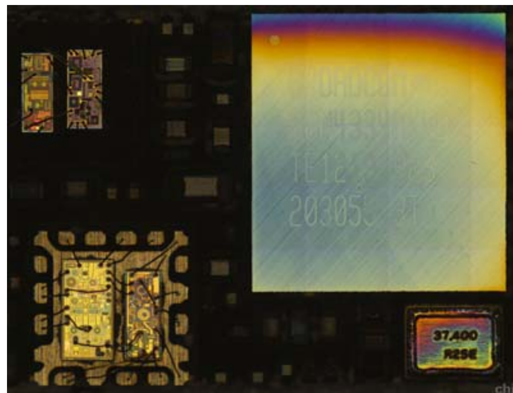


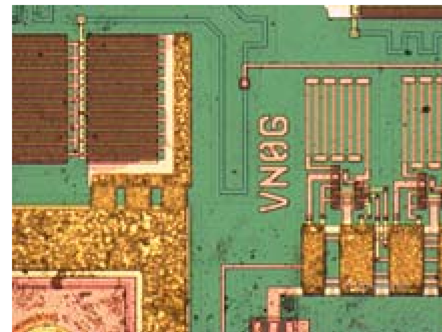
2. New materials with improved transport characteristics:

n-channel: Si → Strained Si → SiGe → InGaAs

p-channel: Si → Strained Si → SiGe → Ge → InGaSb

III-V electronics in your pocket!





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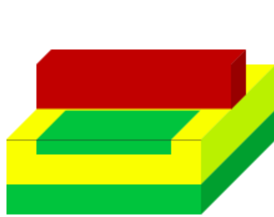
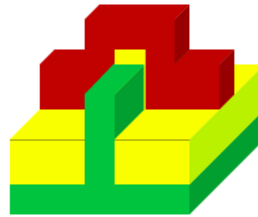
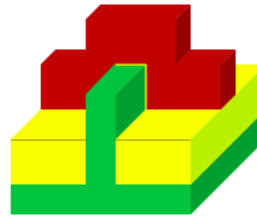
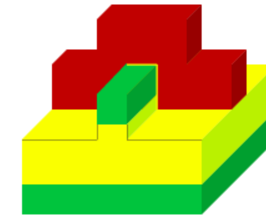


1. Planar InGaAs MOSFET

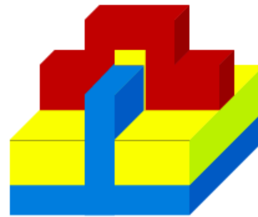




2. InGaAs FinFET



3. InGaAs Gate-All-Around Nanowire MOSFET



4. InGaSb FinFET

Jianqiang Lin

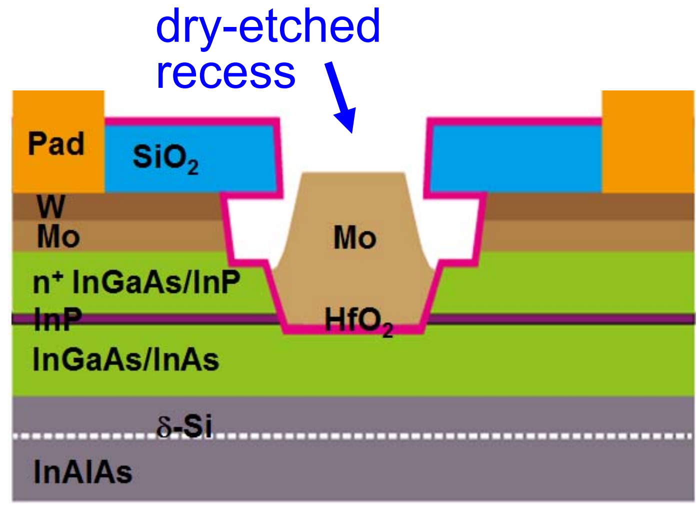
Alon Vardi

Wenjie Lu

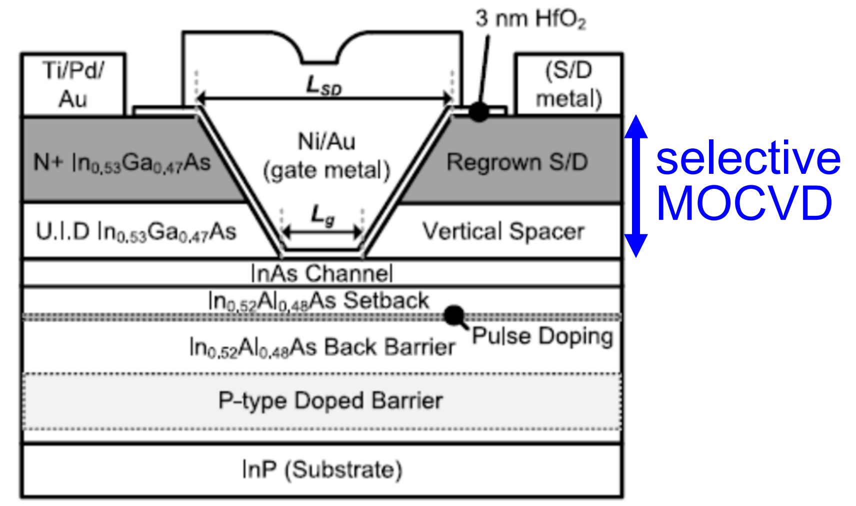
Xin Zhao

1. Self-aligned Planar InGaAs MOSFETs

dry-etched recess



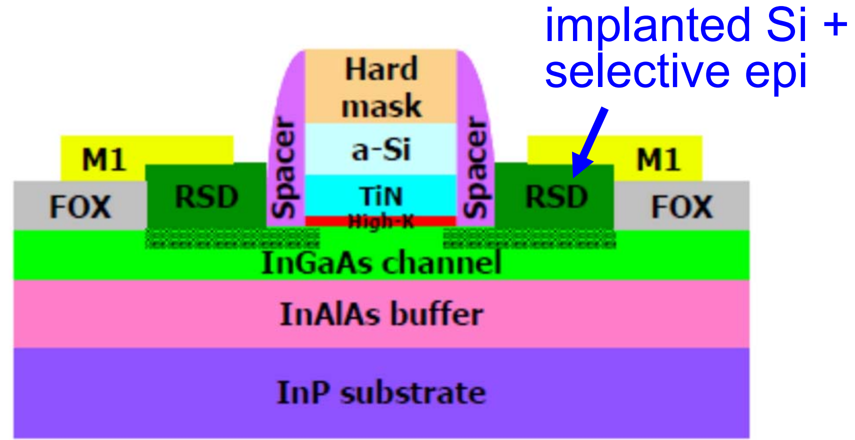
Lin, IEDM 2012, 2013, 2014



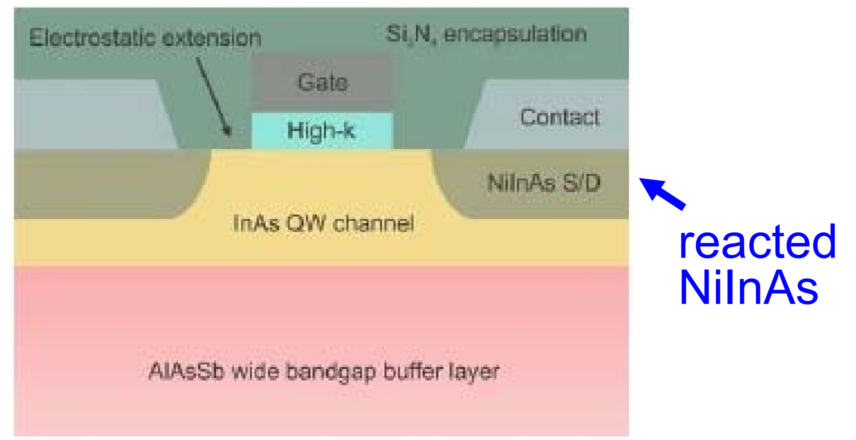
selective MOCVD

Lee, EDL 2014; Huang, IEDM 2014

implanted Si + selective epi



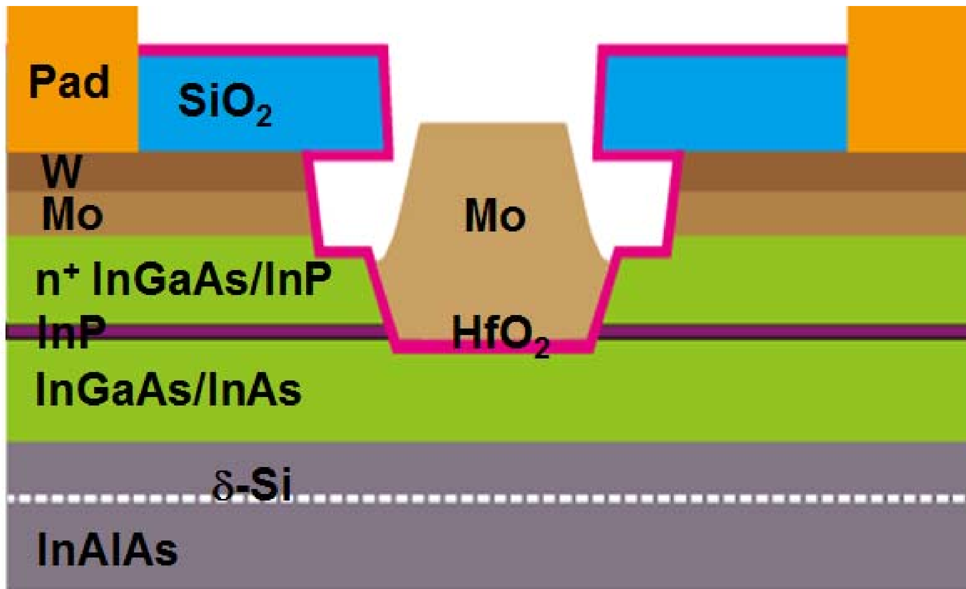
Sun, IEDM 2013, 2014

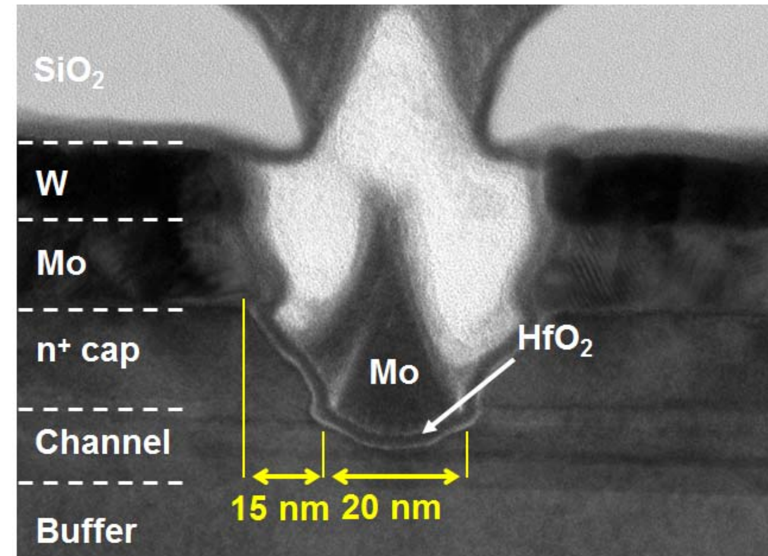


reacted NiInAs

Chang, IEDM 2013

Self-aligned Planar InGaAs MOSFETs @ MIT

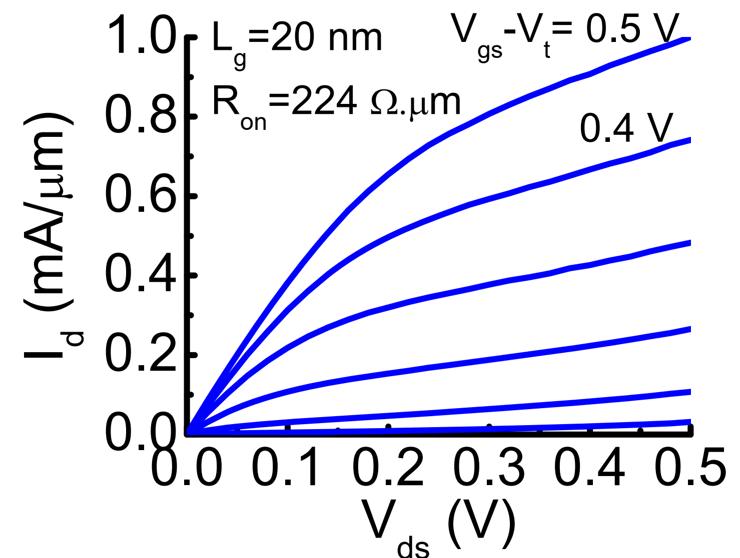




Lin, IEDM 2012, 2013, 2014

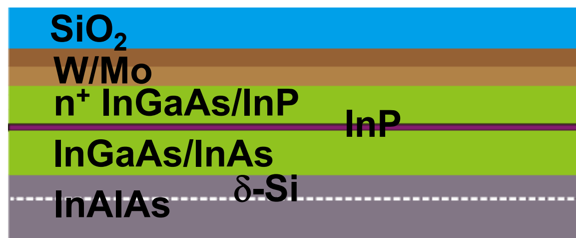
Recess-gate process:

- CMOS-compatible
- Refractory ohmic contacts
- Extensive use of RIE

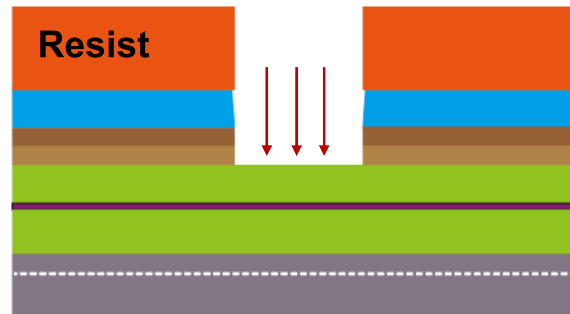


Fabrication process

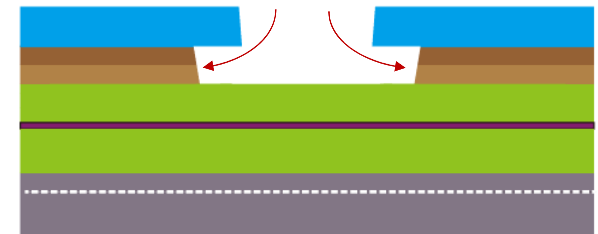
Mo/W ohmic contact + SiO_2 hardmask



SF_6, CF_4 anisotropic RIE

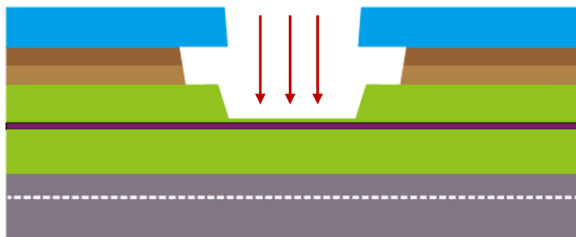


CF_4:O_2 isotropic RIE

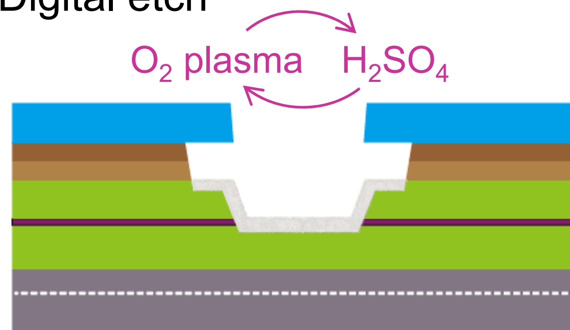


Waldron, IEDM 2007

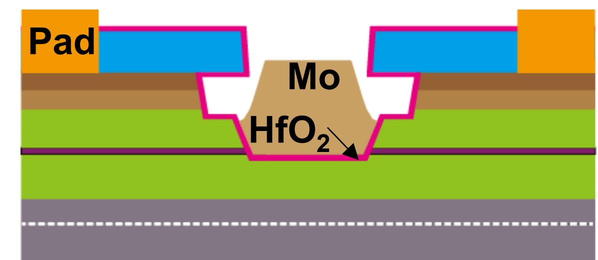
Cl_2:N_2 anisotropic RIE



Digital etch



Finished device

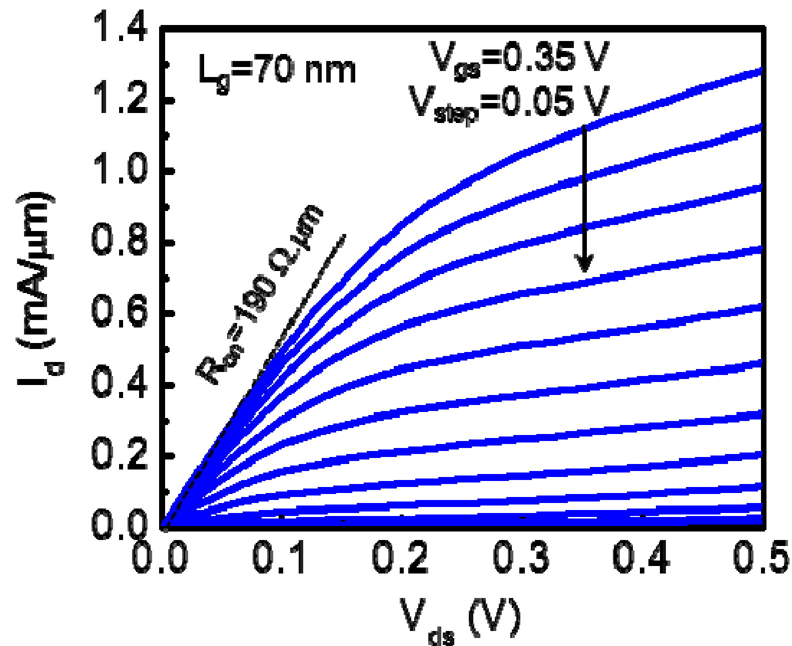


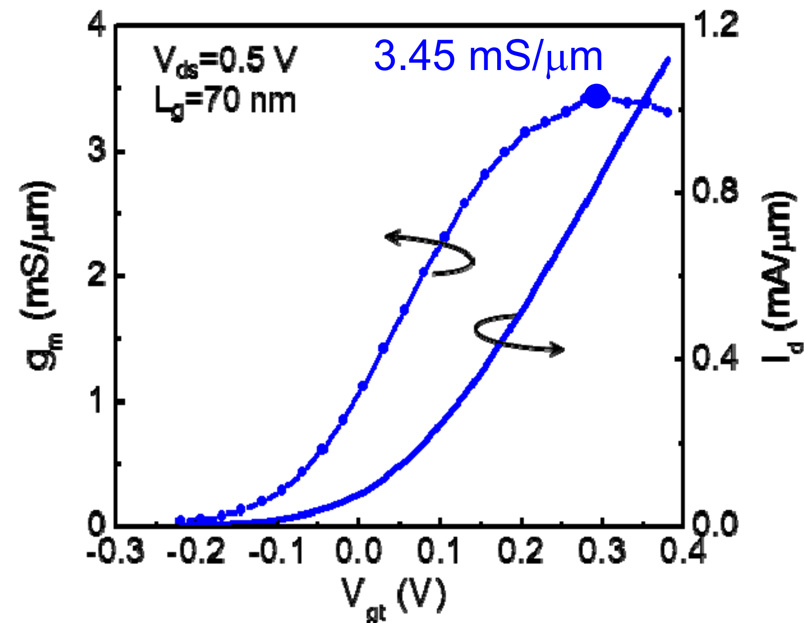
Lin, EDL 2014

- Ohmic contact first, gate last
- Precise control of vertical (~1 nm), lateral (~5 nm) dimensions
- MOS interface exposed late in process

Highest performance InGaAs MOSFET

- Channel: $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$ (t_{ch}=9 nm)
- Gate oxide: HfO_2 (2.5 nm, EOT~ 0.5 nm)





L_g=70 nm:

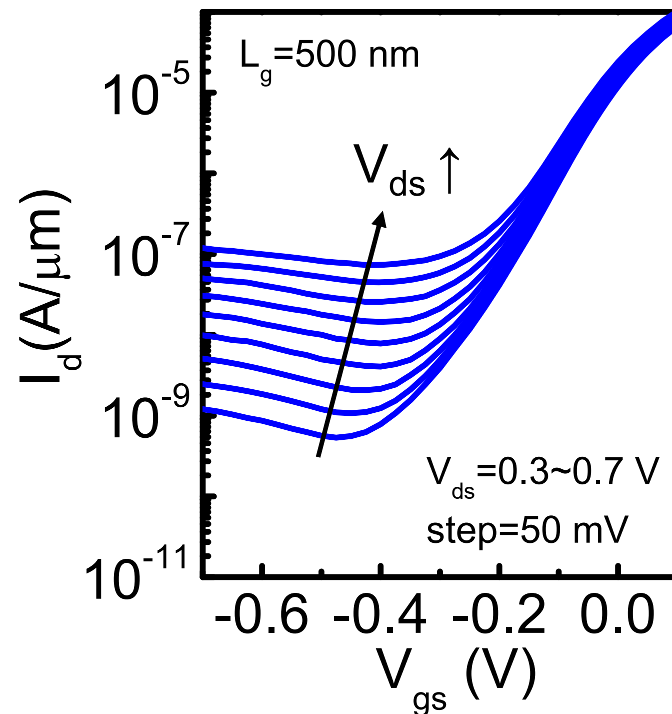
Exceeds best HEMT!

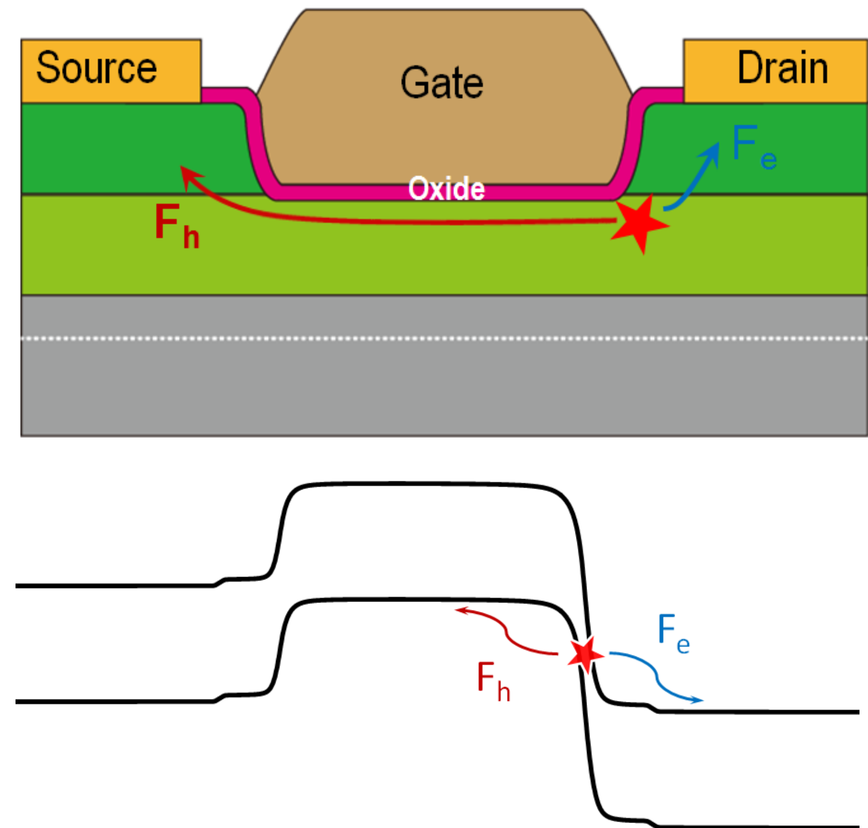
- Record $g_{m,max}$ = 3.45 mS/μm at V_{ds}= 0.5 V
- R_{on} = 190 Ω.μm

Lin, EDL 2016

Excess OFF-state current

Transistor fails to turn off:



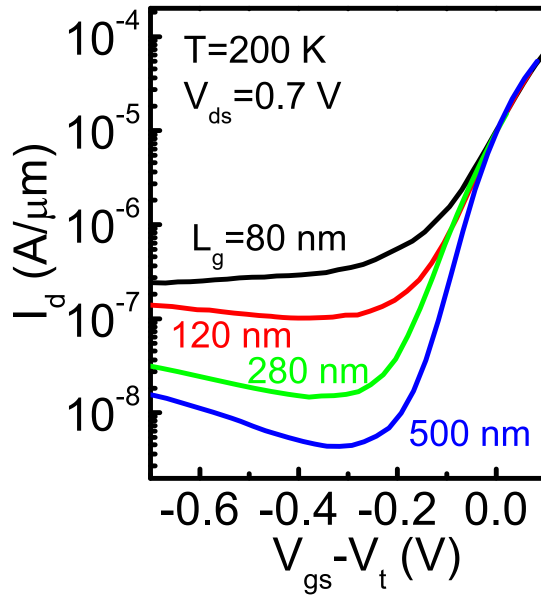


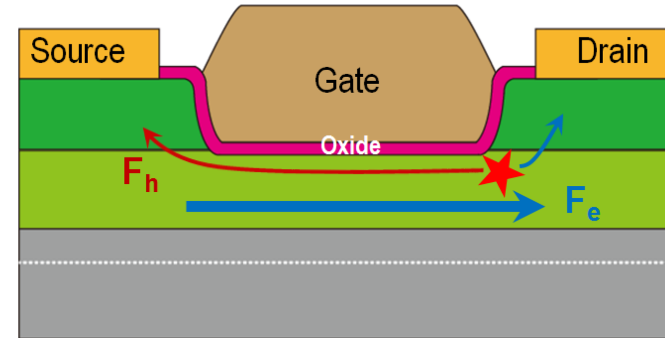
OFF-state current enhanced with V_{ds}

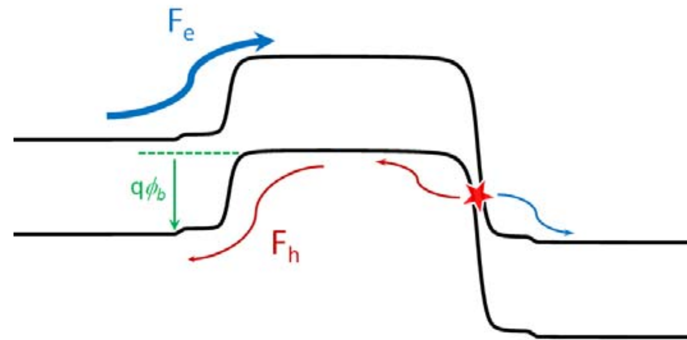
→ *Band-to-Band Tunneling (BTBT) or Gate-Induced Drain Leakage (GIDL)*

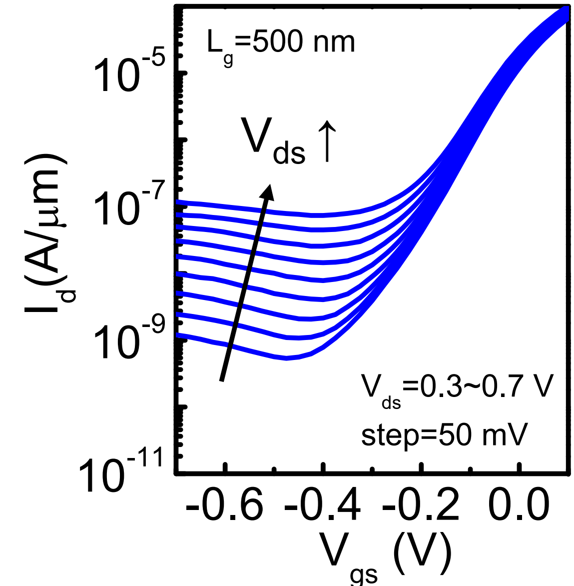
Lin, IEDM 2013

Excess OFF-state current

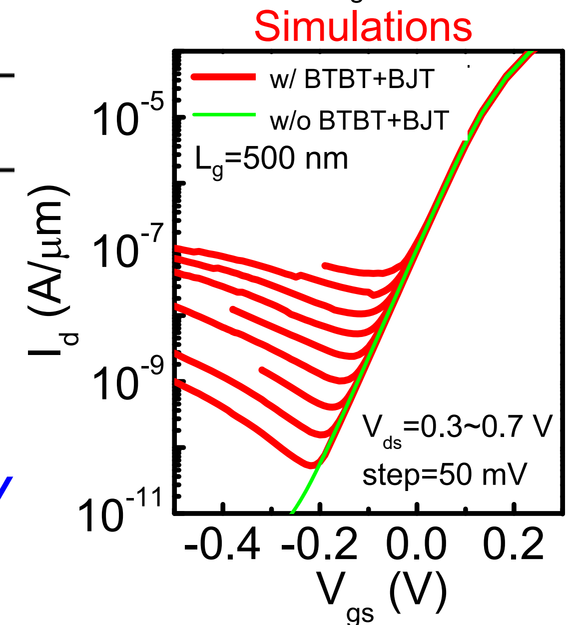








Simulations



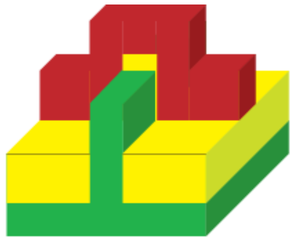
Lin, EDL 2014

Lin, TED 2015

L_g↓ → OFF-state current ↑

→ *bipolar gain effect due to floating body*

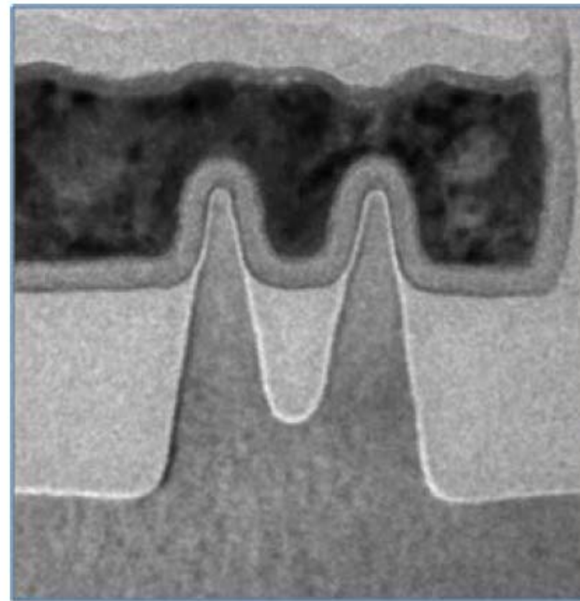
2. InGaAs FinFETs



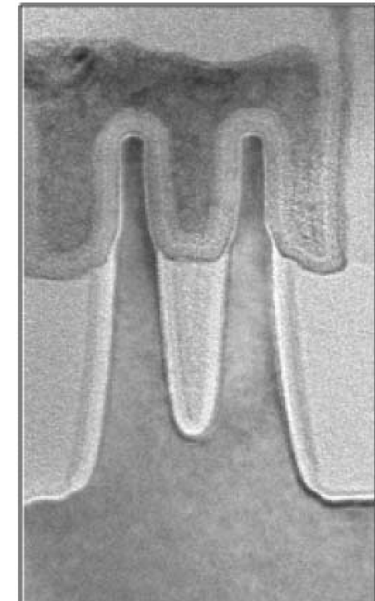
Double-gate MOSFET

Tri-gate MOSFET

Intel Si Trigate MOSFETs

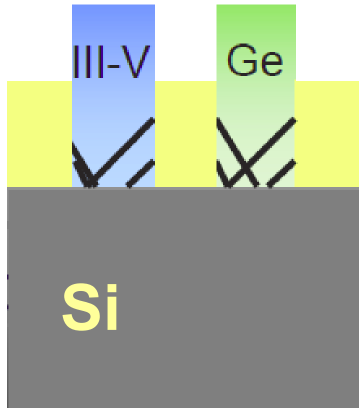


22 nm Process

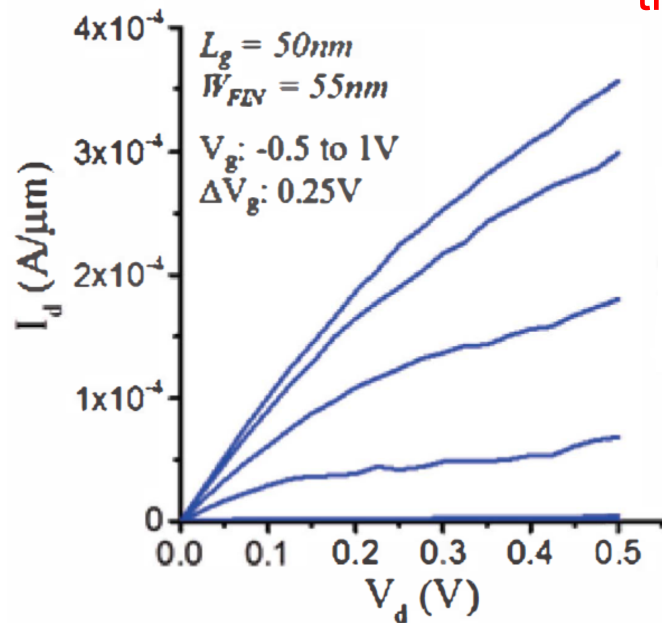


14 nm Process

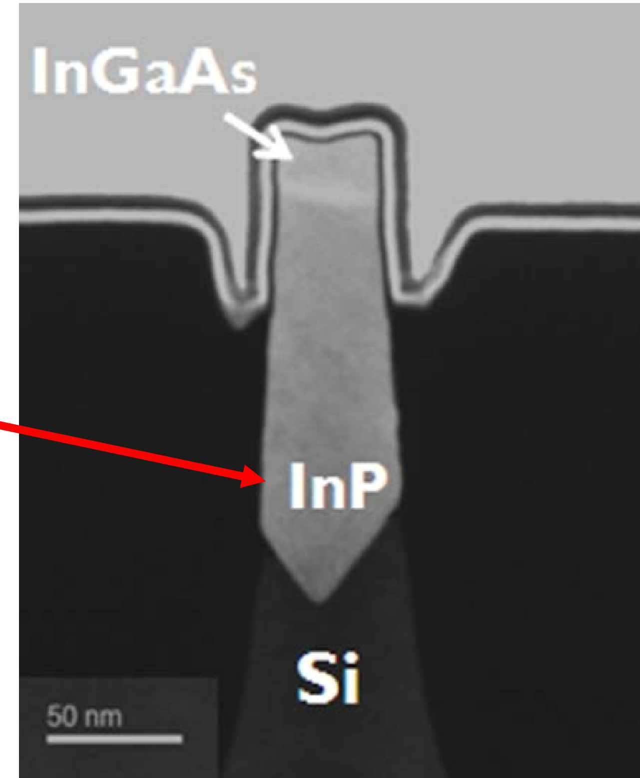
Bottom-up InGaAs FinFETs



Aspect-Ratio Trapping
Fiorenza, ECST 2010

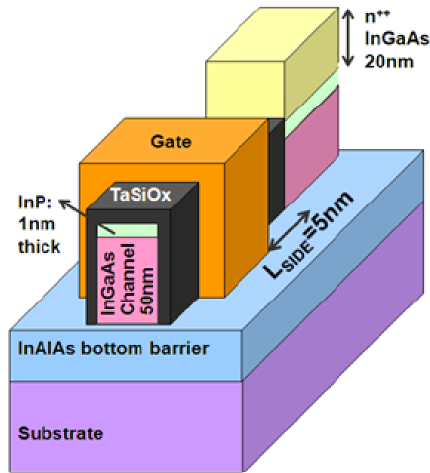


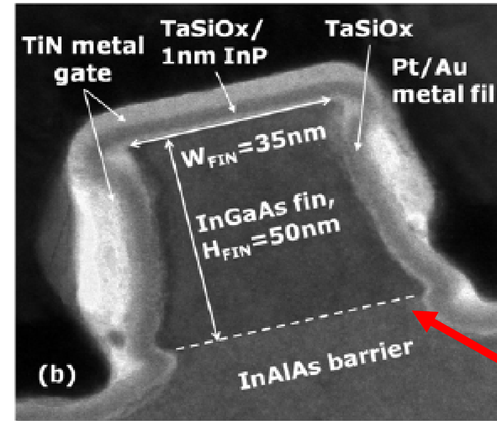
Epi-grown fin inside trench



Waldron, VLSI Tech 2014

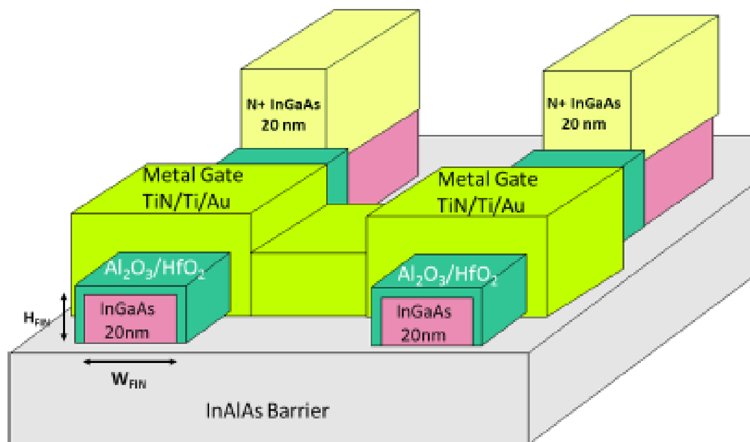
Top-down InGaAs FinFETs

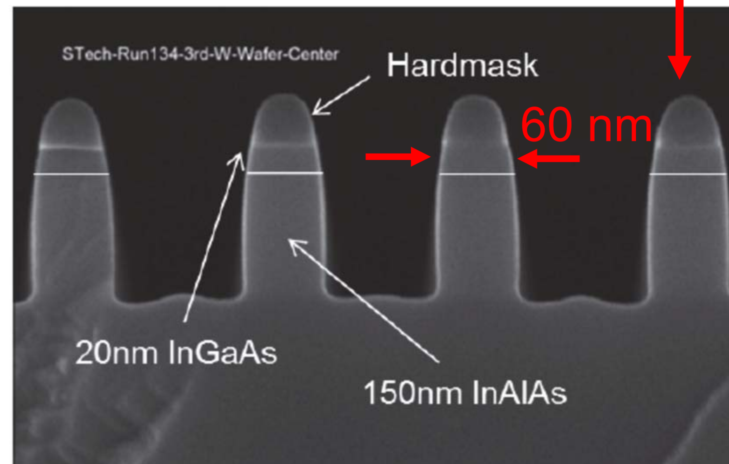




dry-etched fins

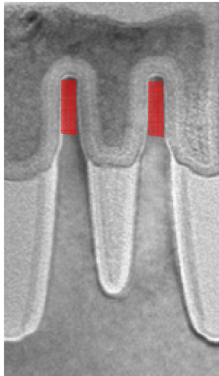
Radosavljevic, IEDM 2010





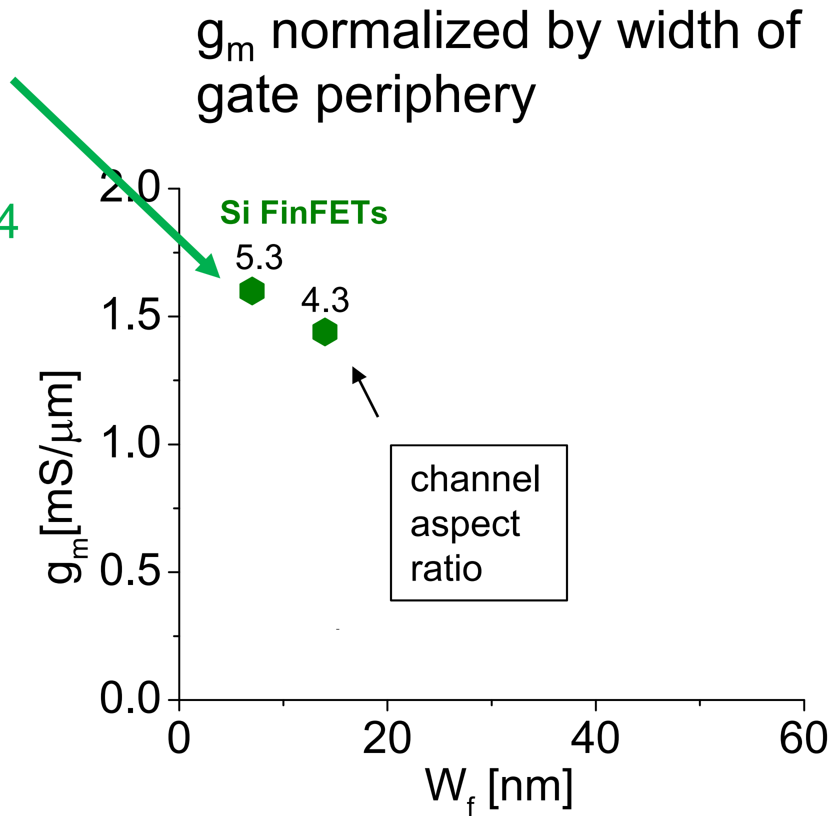
Kim, IEDM 2013

FinFET benchmarking



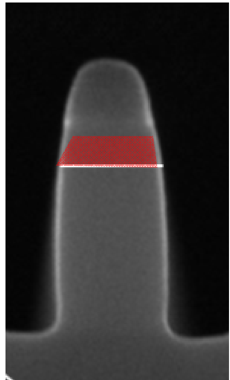
Natarajan, IEDM 2014

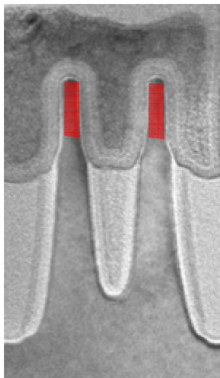
g_m normalized by width of gate periphery



- State-of-the-art Si FinFETs: W_f=7 nm

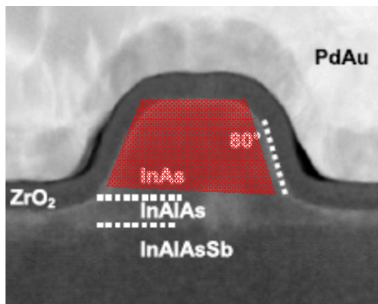
FinFET benchmarking





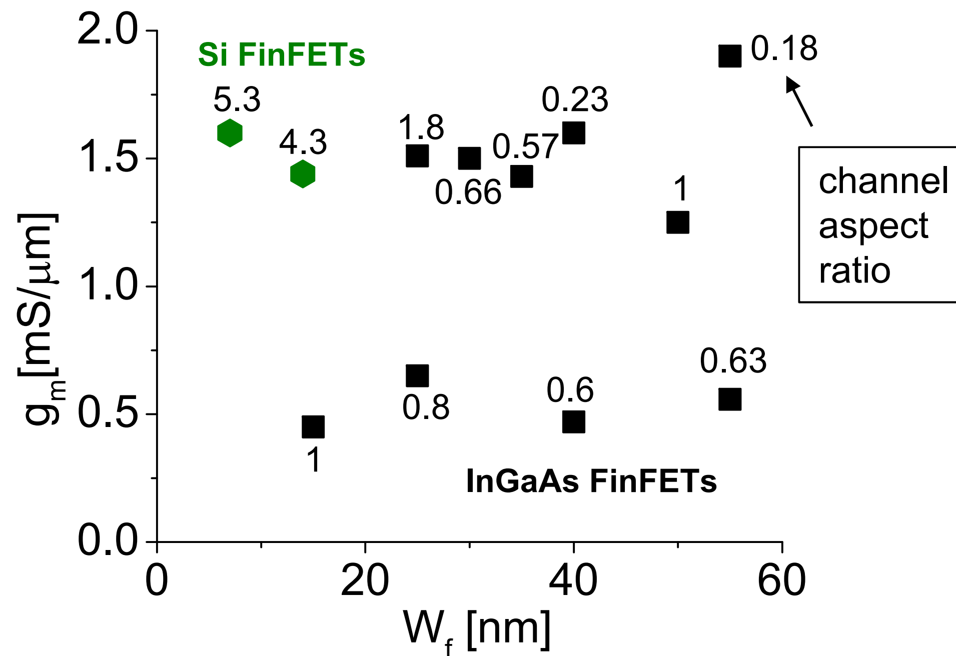
Natarajan, IEDM 2014

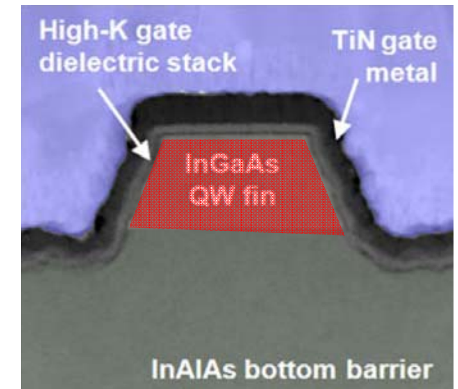
Kim, IEDM 2013



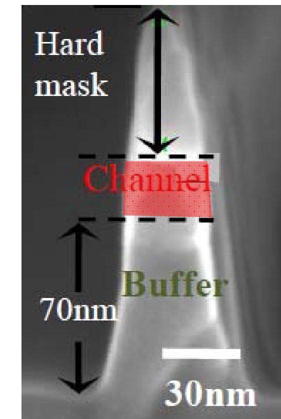
Oxland, EDL 2016

g_m normalized by width of gate periphery





Radosavljevic, IEDM 2011

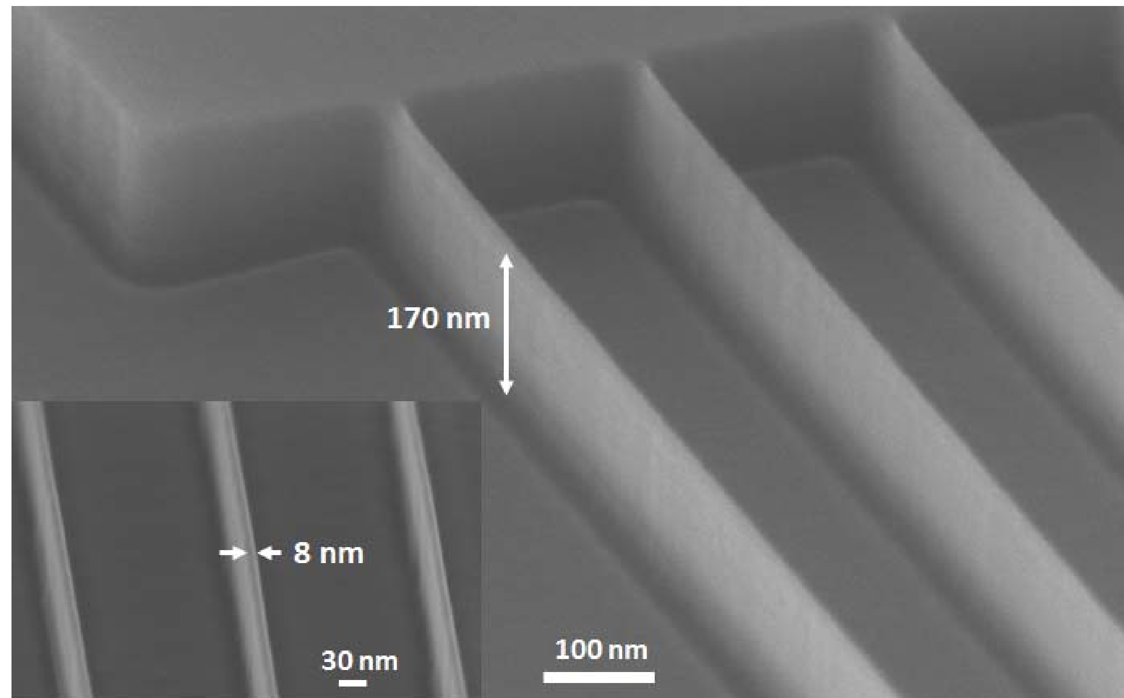


Thathachary, VLSI 2015

- Narrowest InGaAs FinFET fin: W_f=15 nm
- Best channel aspect ratio of InGaAs FinFET: 1.8
- g_m much lower than planar InGaAs MOSFETs

InGaAs FinFETs @ MIT

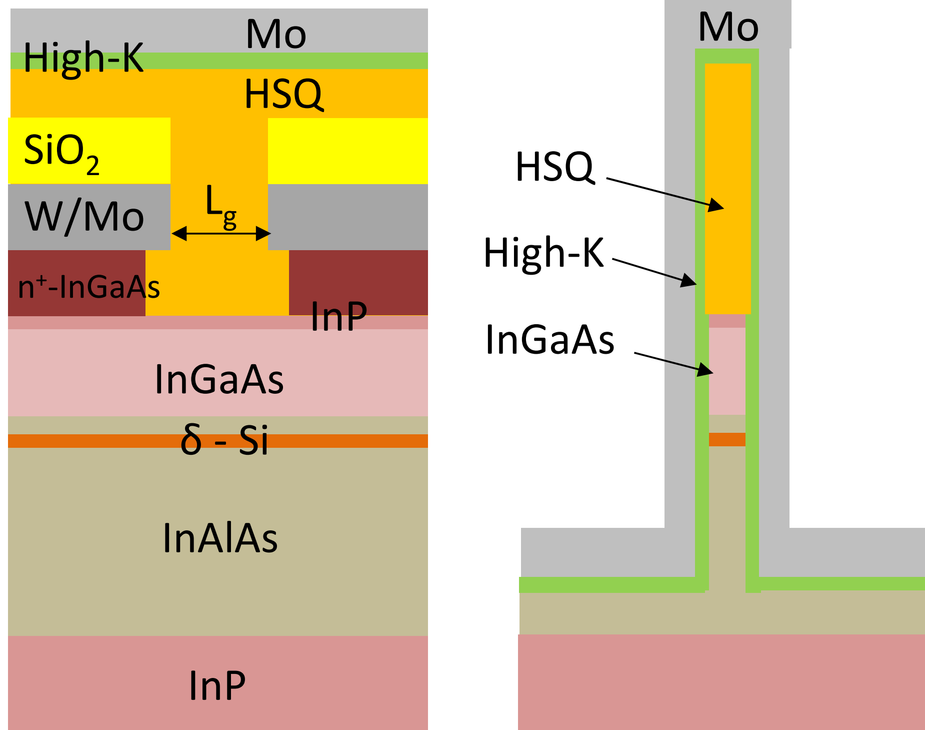
Key enabling technologies: $BCl_3/SiCl_4/Ar$ RIE + digital etch

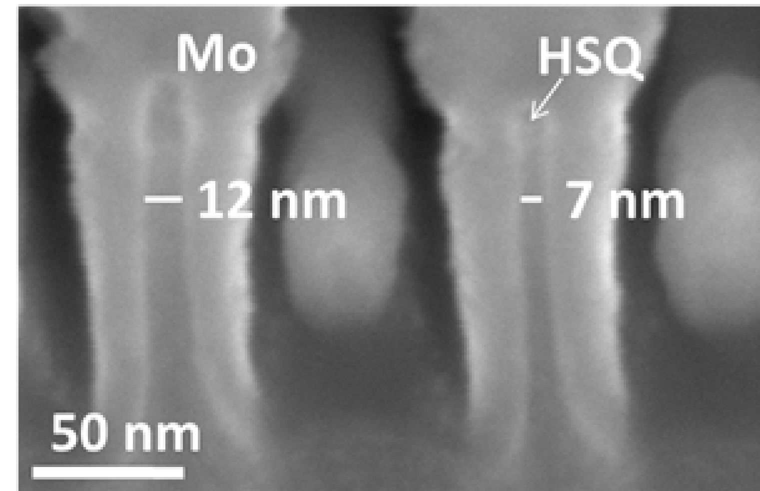


- Sub-10 nm fin width
- Aspect ratio > 20
- Vertical sidewalls

Vardi,
DRC 2014,
EDL 2015,
IEDM 2015

InGaAs FinFETs @ MIT



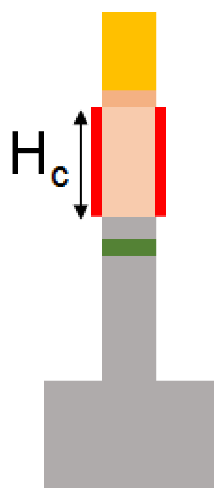


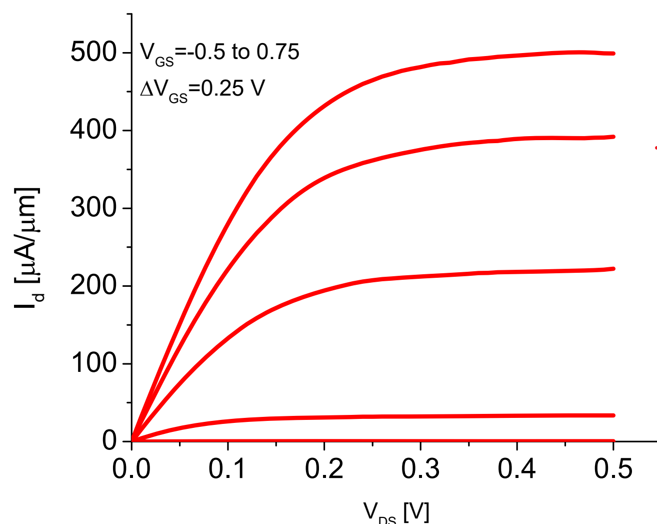
Vardi, VLSI Tech 2016
Vardi, EDL 2016

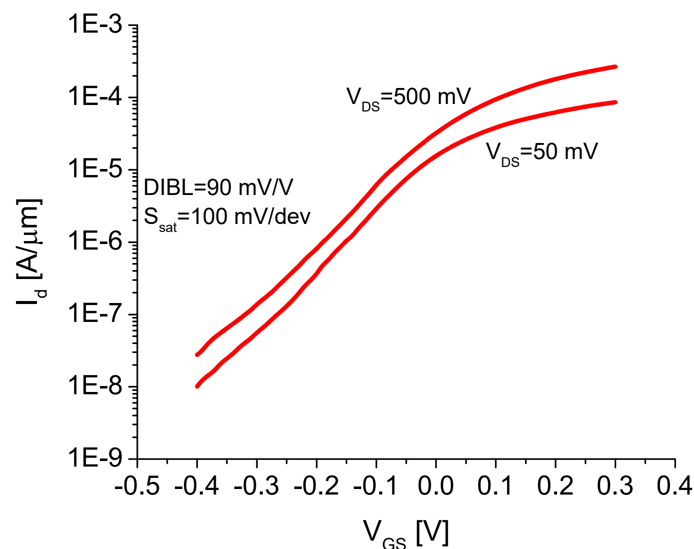
- CMOS compatible process
- Mo contact-first process
- Fin etch mask left in place → double-gate MOSFET

Most aggressively scaled FinFET

W_f=7 nm, L_g=30 nm, H_c=40 nm (AR=5.7), EOT=0.6 nm:



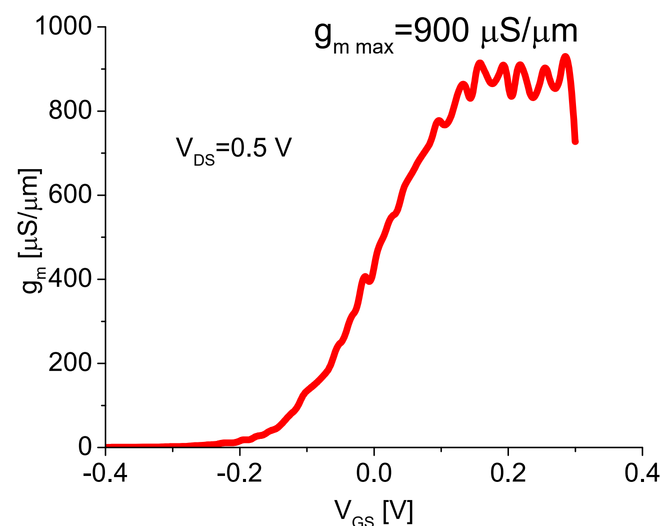




Current normalized by $2xH_c$

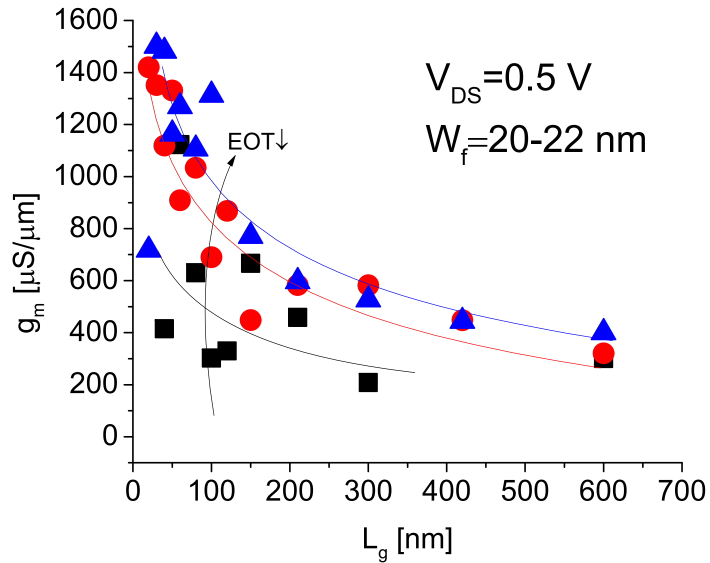
At V_{DS}=0.5 V:

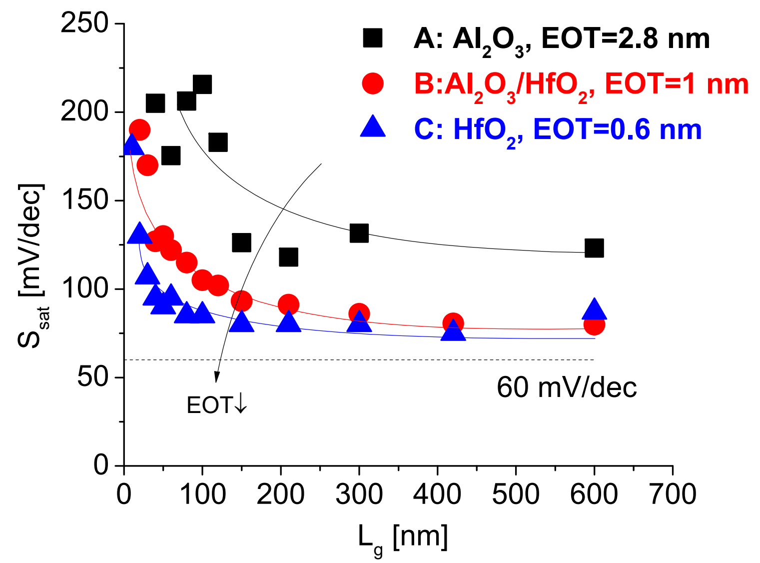
- g_m=900 µS/µm
- R_{on}=320 Ω.µm
- S_{sat}=100 mV/dec

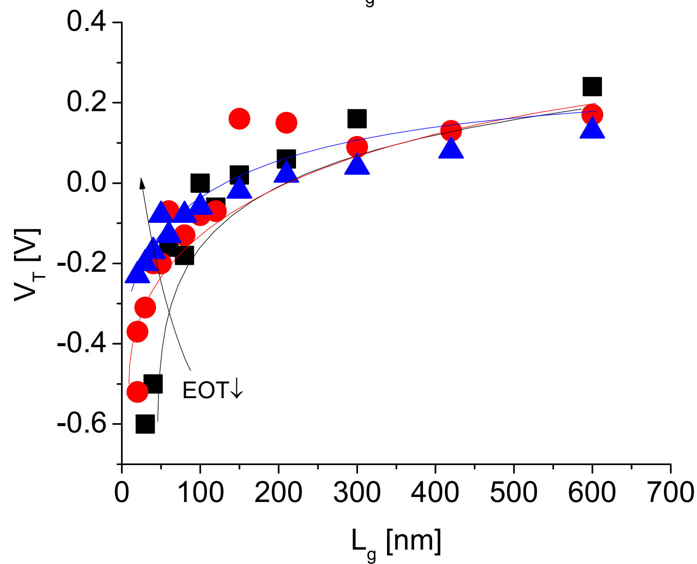


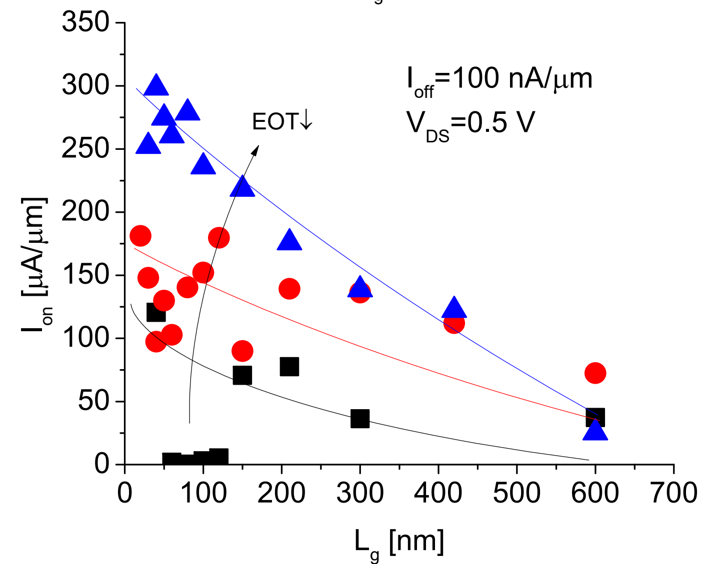
Vardi, EDL 2016

L_g and EOT scaling



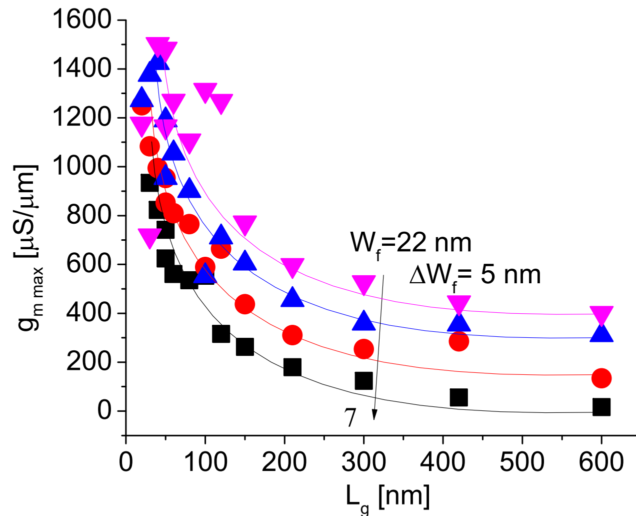


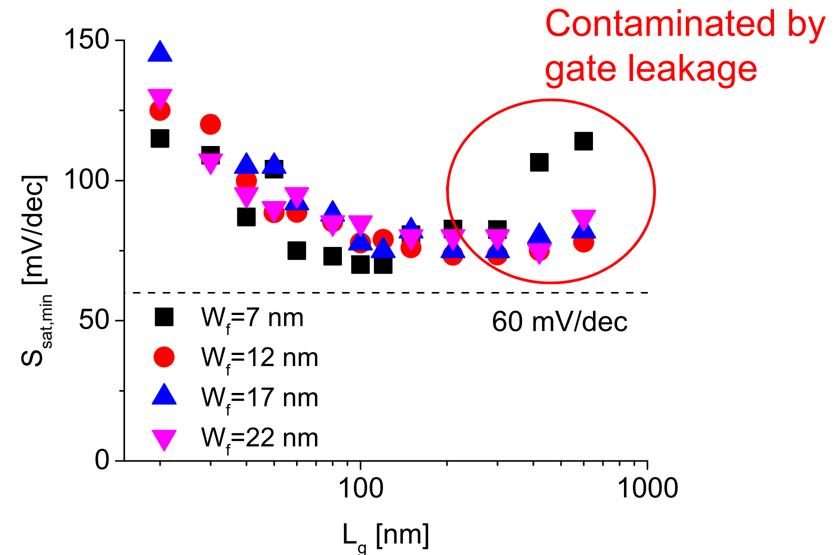


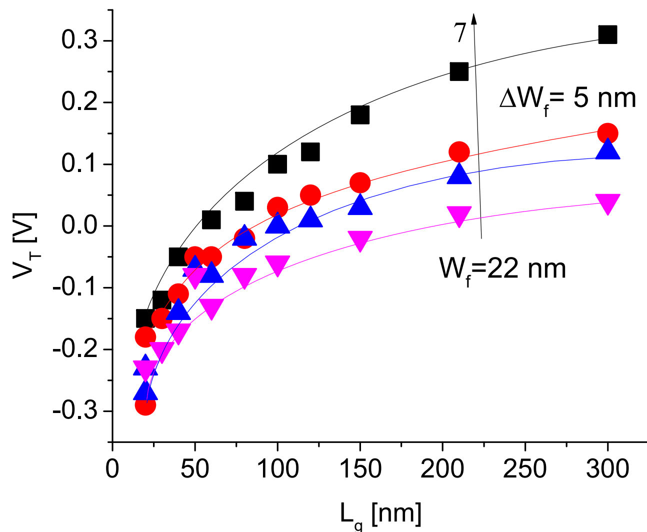


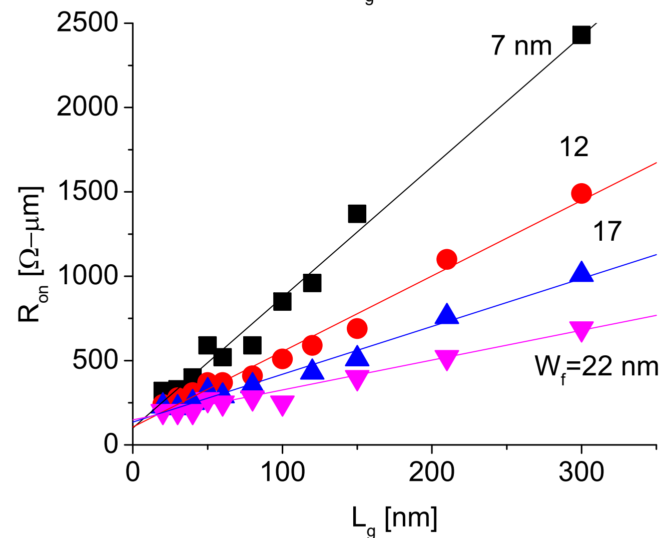
Classical scaling with L_g and EOT

Fin width scaling (EOT=0.6 nm)





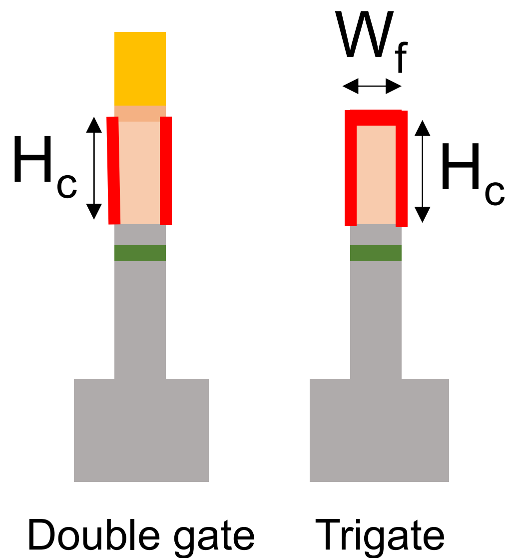


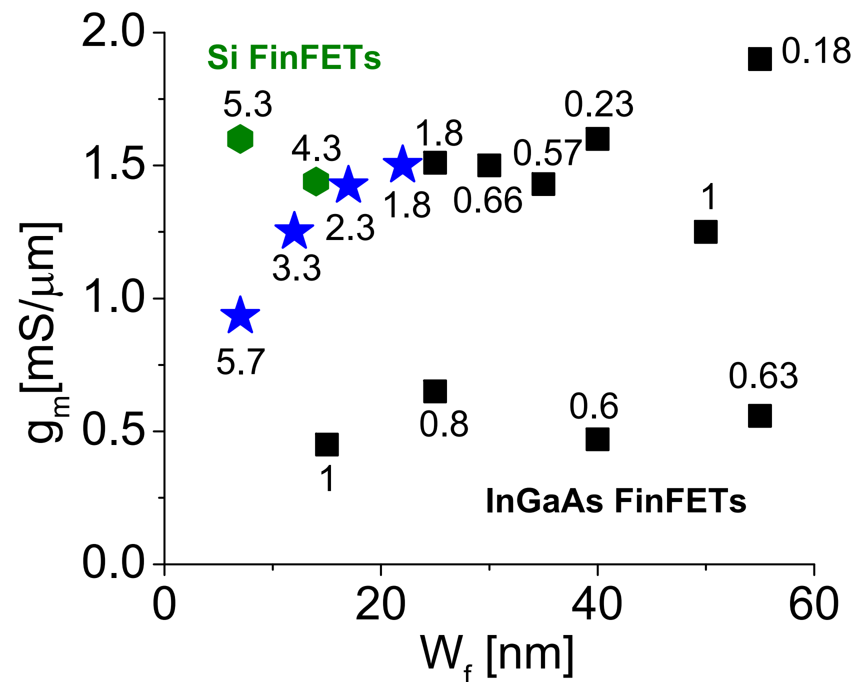


- Non-ideal fin width scaling
- High D_{it} (~5×10^{12} $cm^{-2}.eV^{-1}$); mobility degradation; line edge roughness

InGaAs FinFETs: g_m benchmarking

g_m normalized by width of gate periphery:

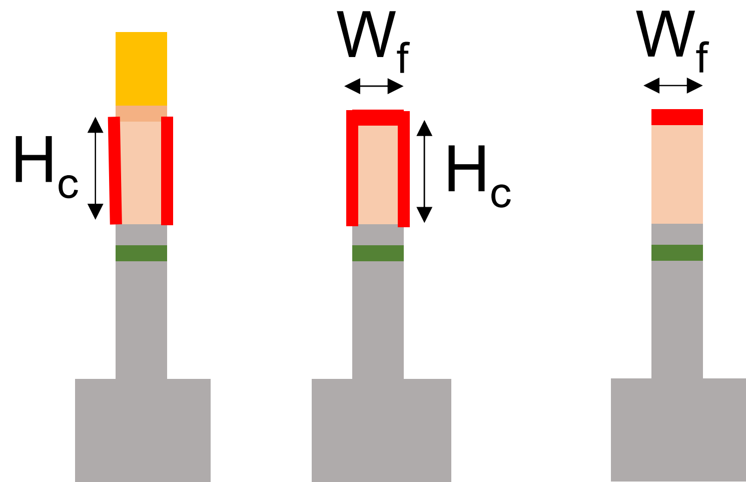




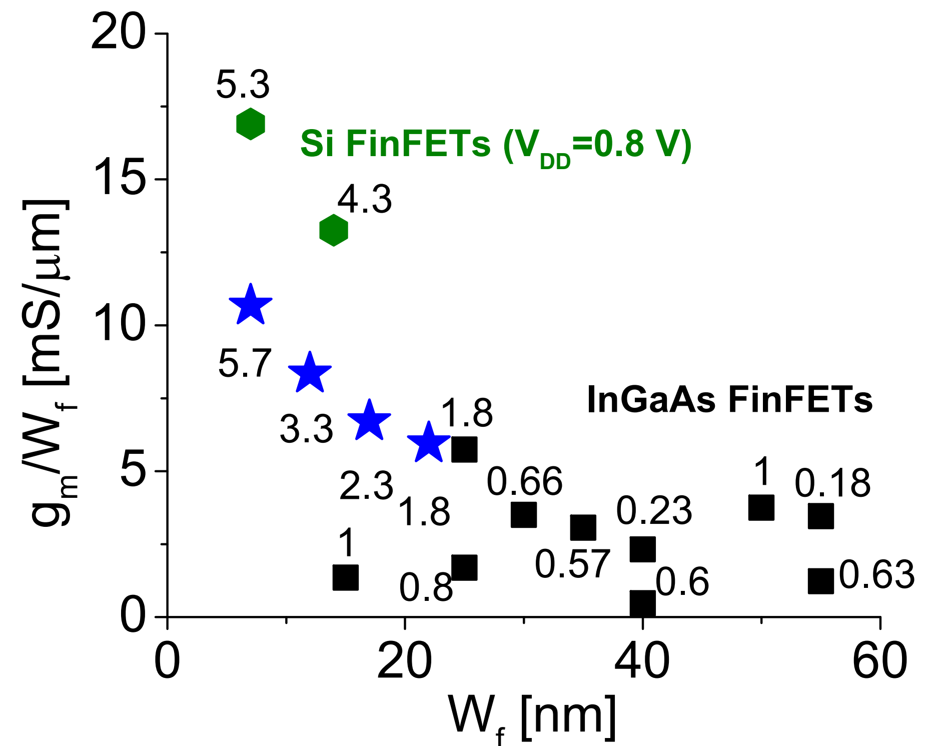
- First InGaAs FinFETs with W_f<10 nm
- Record results for InGaAs FinFETs with W_f < 25 nm
- Still short of Si FinFETs (though they operate at V_{DD}=0.8 V)

InGaAs FinFETs: g_m benchmarking

g_m normalized by fin width (FOM for density):



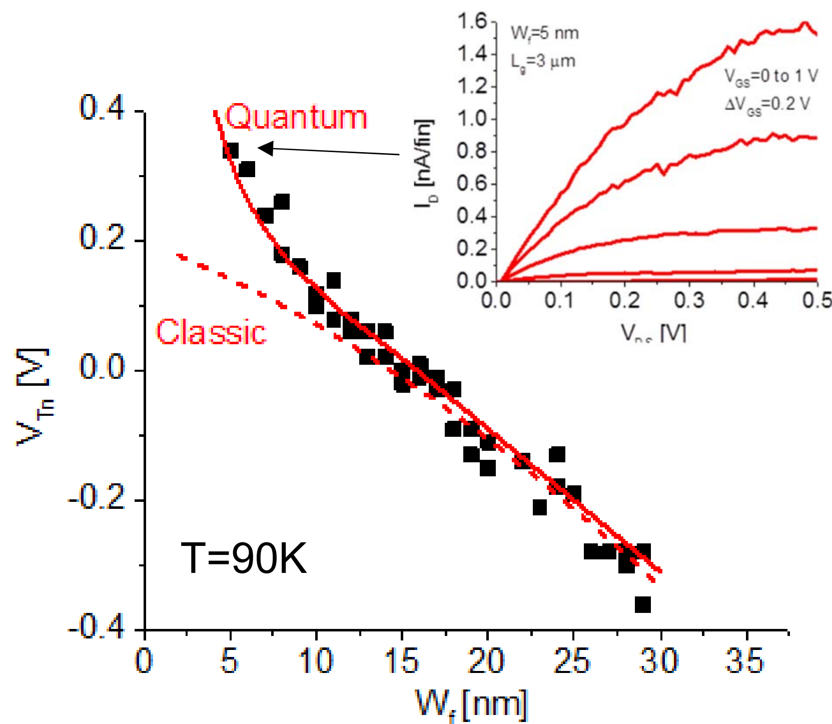
Vardi, EDL 2016

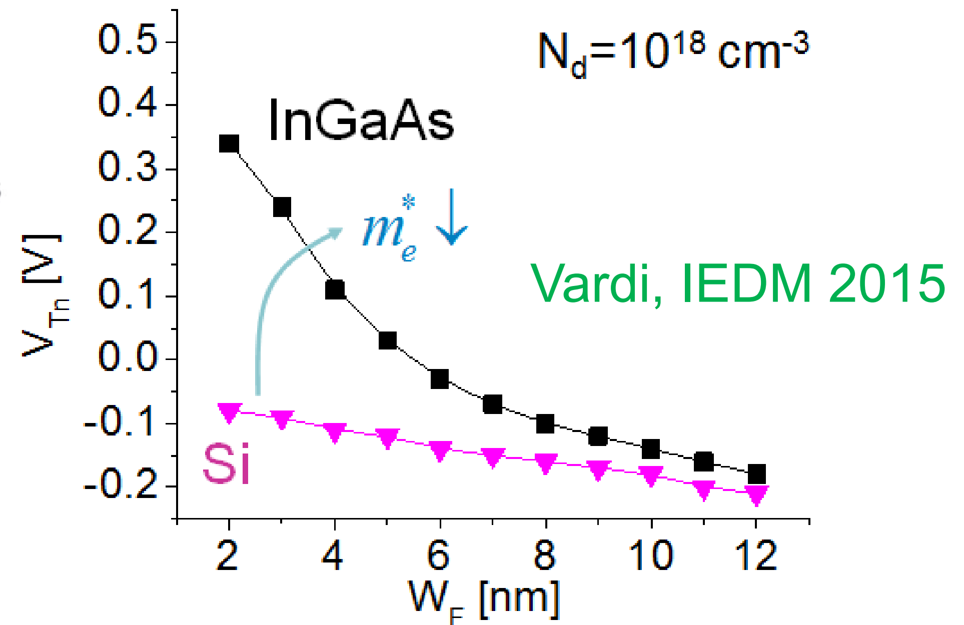


Doubled g_m/W_f over earlier InGaAs FinFETs

Impact of fin width on V_T

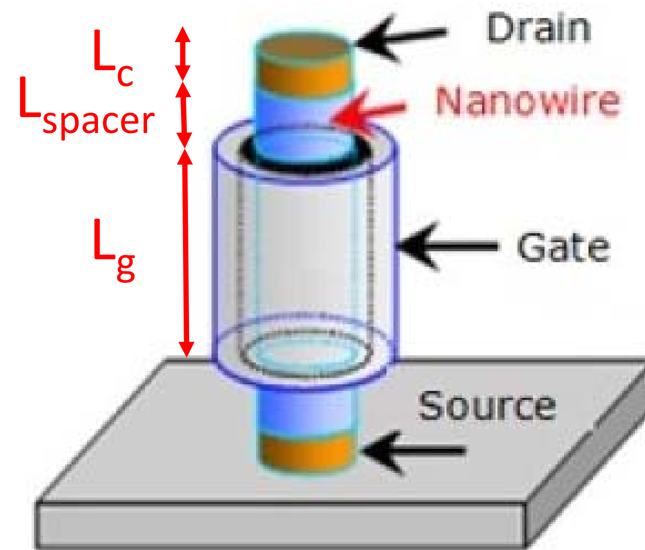
InGaAs doped-channel FinFETs: 50 nm thick, N_D~10^{18} cm^{-3}





- Strong V_T sensitivity for W_f < 10 nm; much worse than Si
- Due to quantum effects
- Big concern for future manufacturing

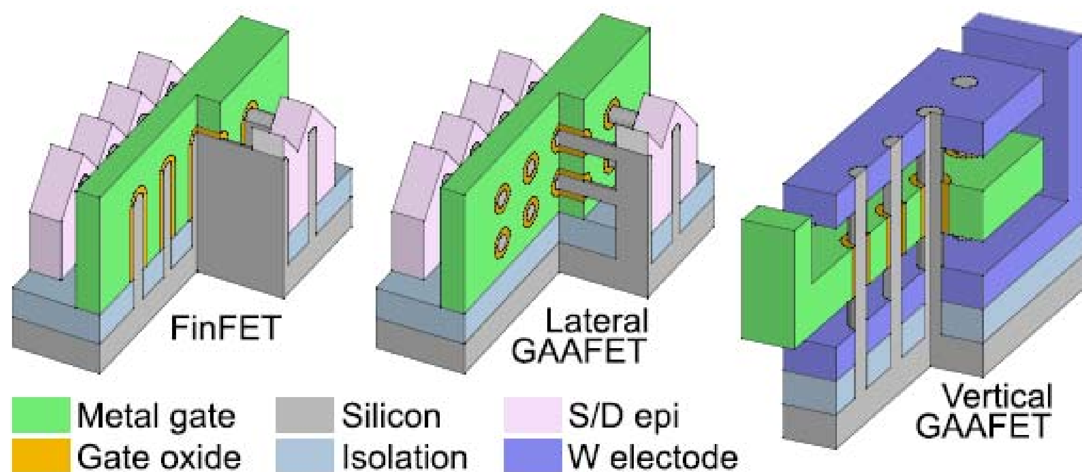
3. Vertical nanowire MOSFET: ultimate scalable transistor

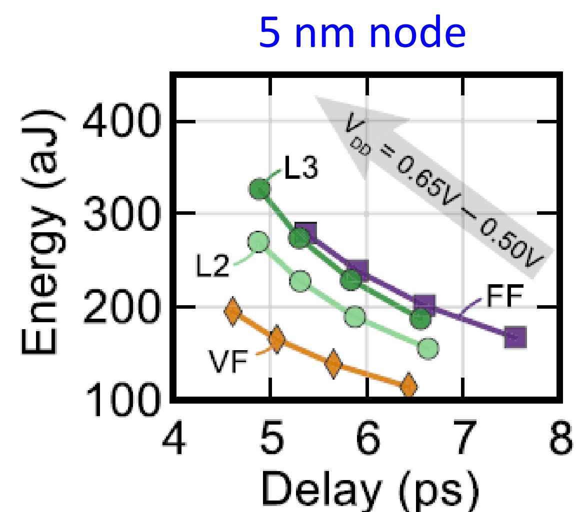


Vertical NW MOSFET:

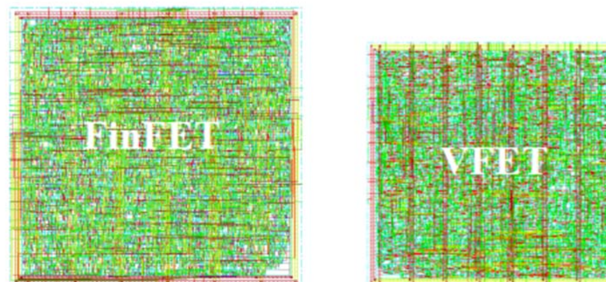
→ uncouples footprint scaling from L_g, L_{spacer}, and L_c scaling

Vertical nanowire MOSFET for 5 nm node





Yakimets, TED 2015
Bao, ESSDERC 2014

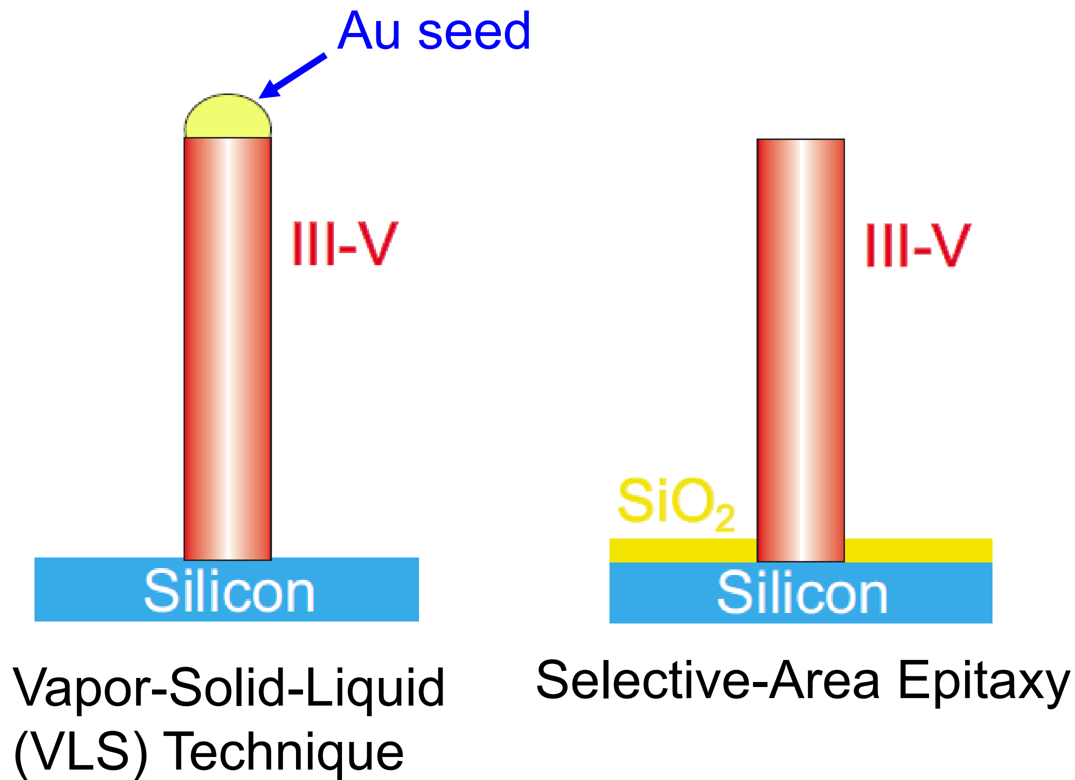


30% area reduction in 6T-SRAM
19% area reduction in 32 bit multiplier

Vertical NW:

→ power, performance and area gains w.r.t. Lateral NW or FinFET

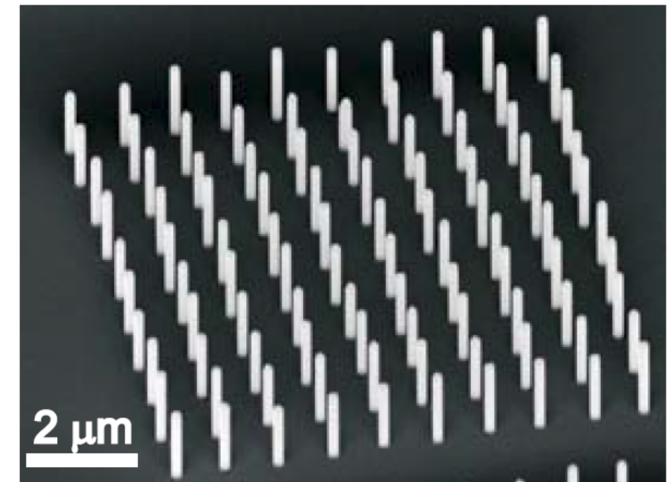
InGaAs Vertical Nanowires on Si by direct growth



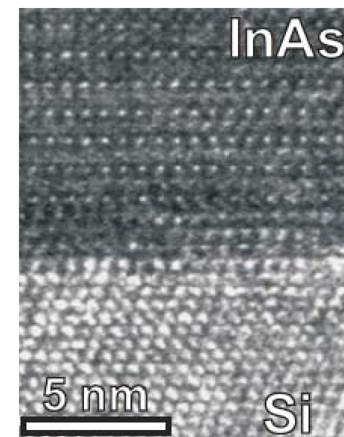
Vapor-Solid-Liquid (VLS) Technique

Selective-Area Epitaxy

Riel, MRS Bull 2014



InAs NWs on Si by SAE



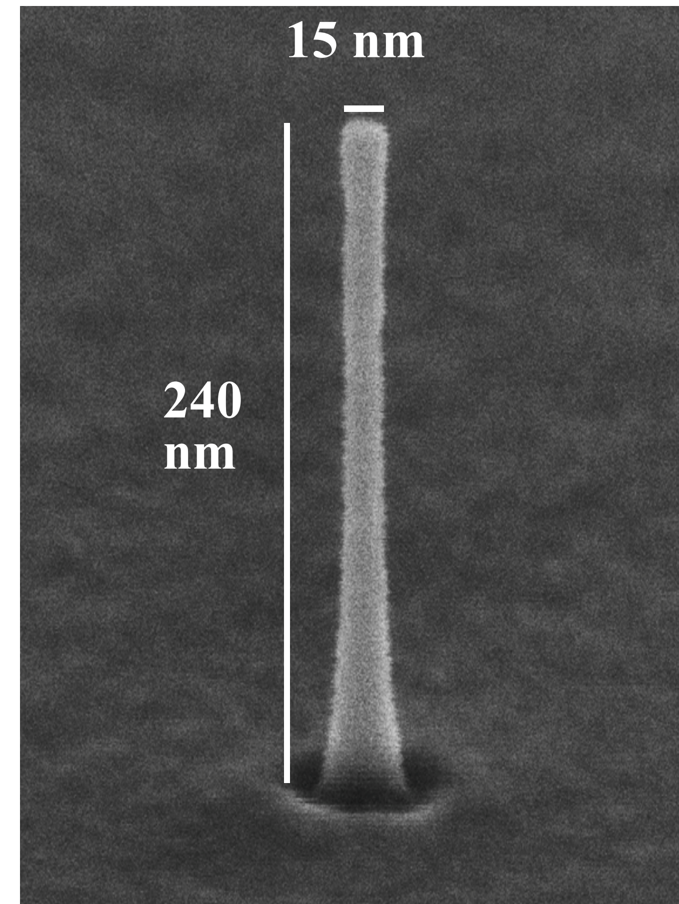
Björk, JCG 2012

InGaAs VNW MOSFETs by top-down approach @ MIT

Key enabling technologies:

- RIE = $BCl_3/SiCl_4/Ar$ chemistry
- Digital Etch (DE) =
  - O_2 plasma oxidation
  - H_2SO_4 oxide removal

- Sub-20 nm NW diameter
- Aspect ratio > 10
- Smooth sidewalls

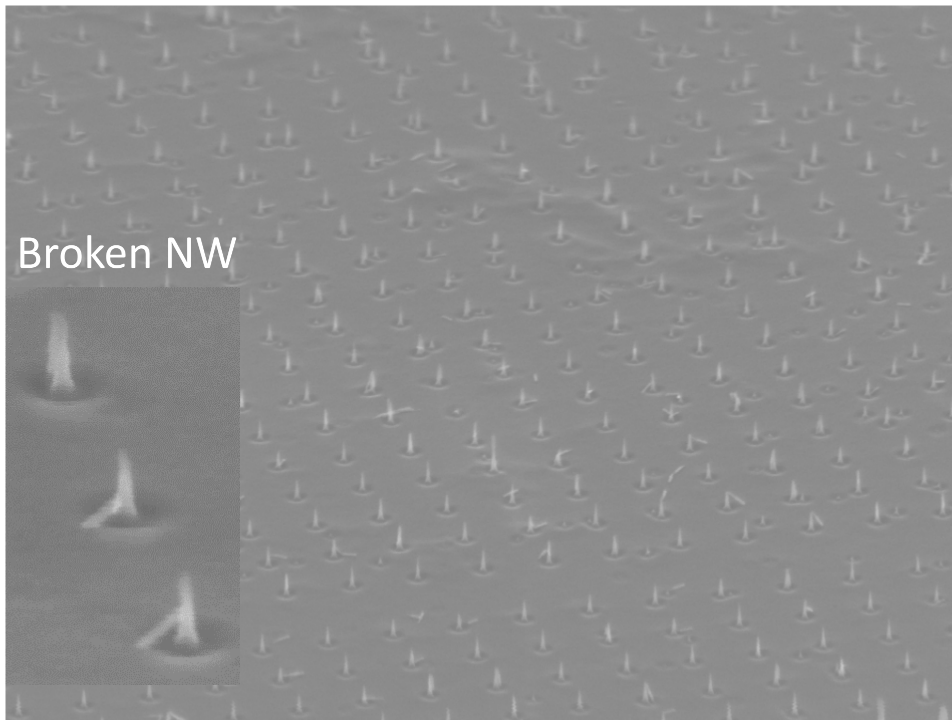


Zhao, EDL 2014

InGaAs VNW Mechanical Stability for D<10 nm

Difficult to reach 10 nm VNW diameter due to breakage

8 nm InGaAs VNWs: Yield = 0%



InGaAs VNW Mechanical Stability for D<10 nm

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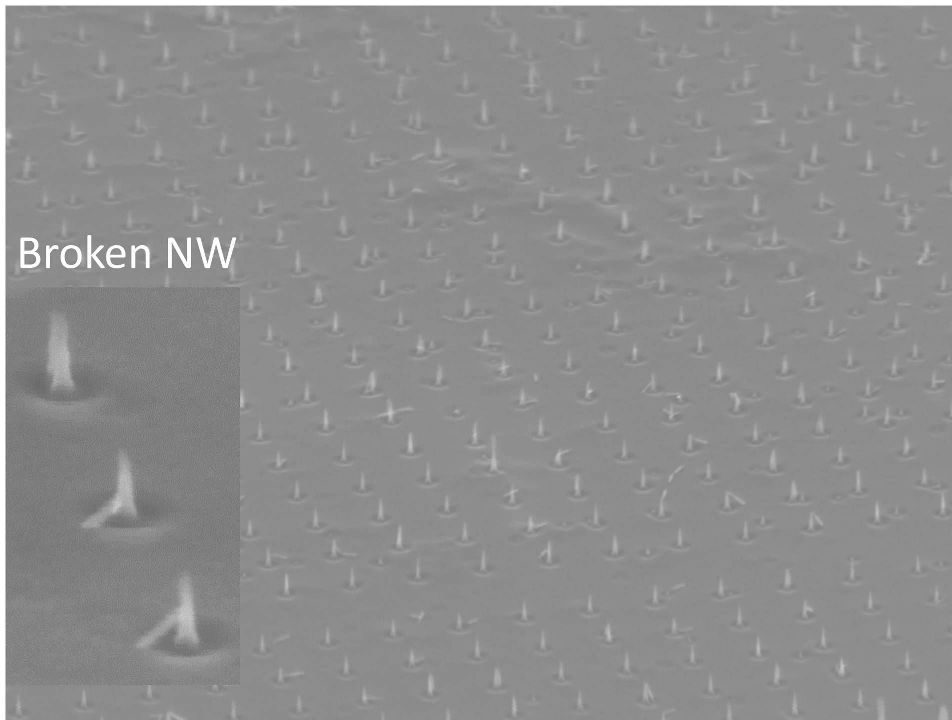


Water-based acid is problem:

Surface tension (mN/m):
- Water: 72
- Methanol: 22
- IPA: 23

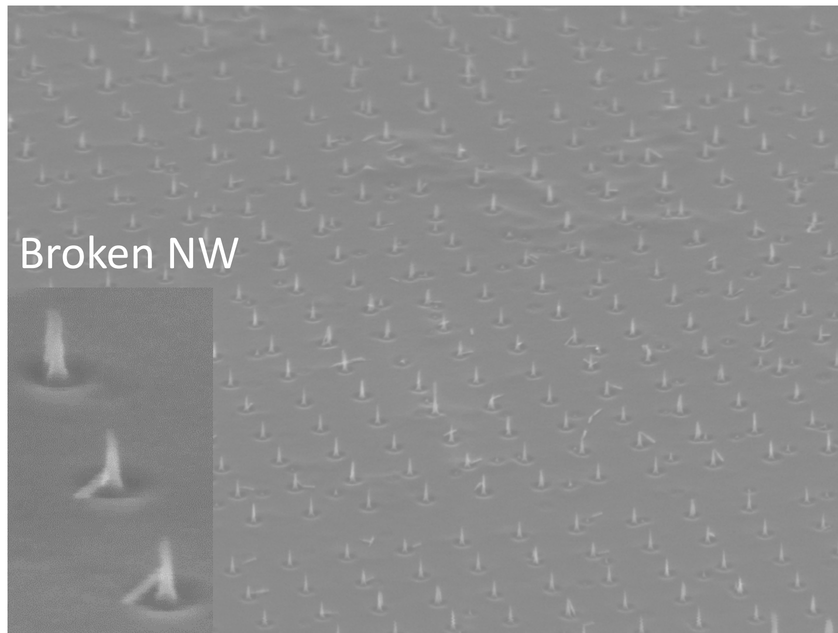
Solution: *alcohol-based digital etch*

Alcohol-Based Digital Etch

8 nm InGaAs VNWs

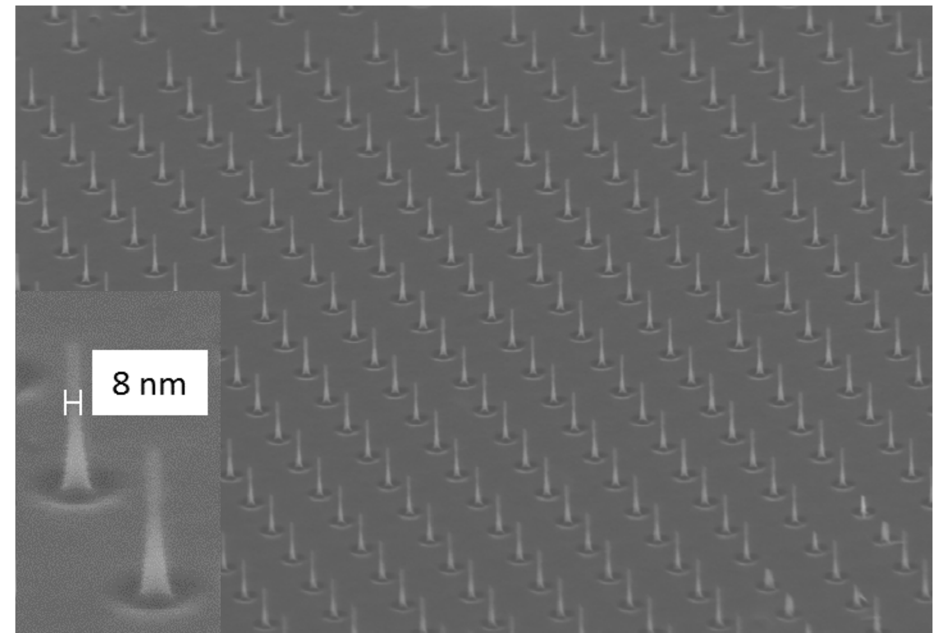
Lu, EDL 2017

10% HCl in DI water
Yield = 0%



Radial etch rate: 1.0 nm/cycle

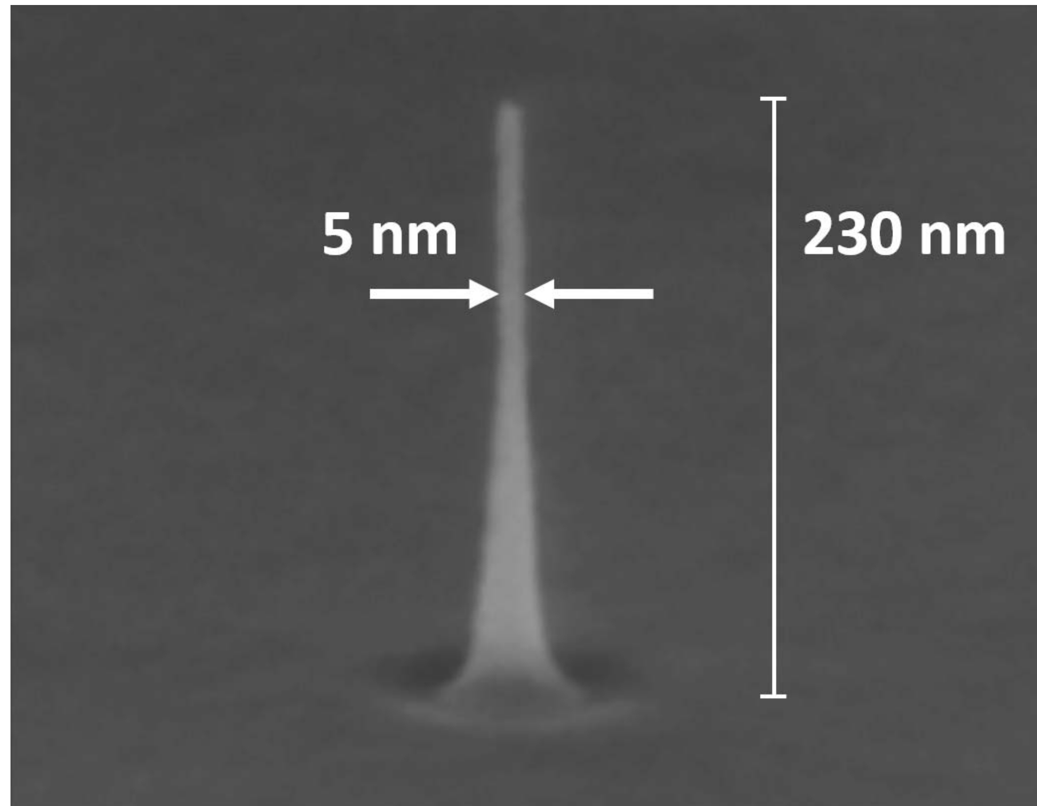
10% HCl in IPA
Yield = 97%



Radial etch rate: 1.0 nm/cycle

Alcohol-based DE enables D < 10 nm

InGaAs Digital Etch

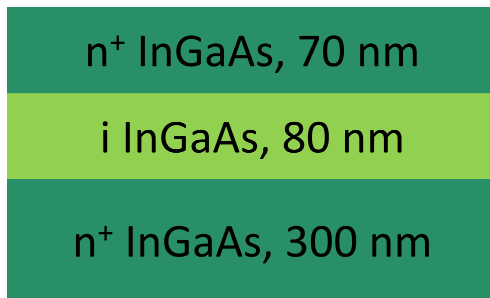


First demonstration of D=5 nm diameter InGaAs VNW
(Aspect Ratio > 40)

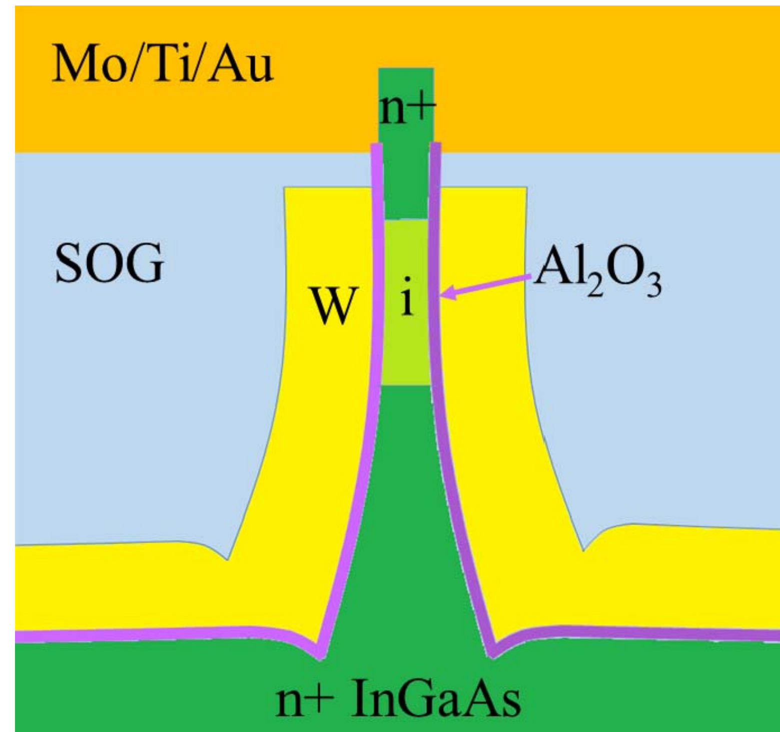
Lu, EDL 2017

InGaAs VNW-MOSFETs by top-down approach @ MIT

Starting heterostructure:



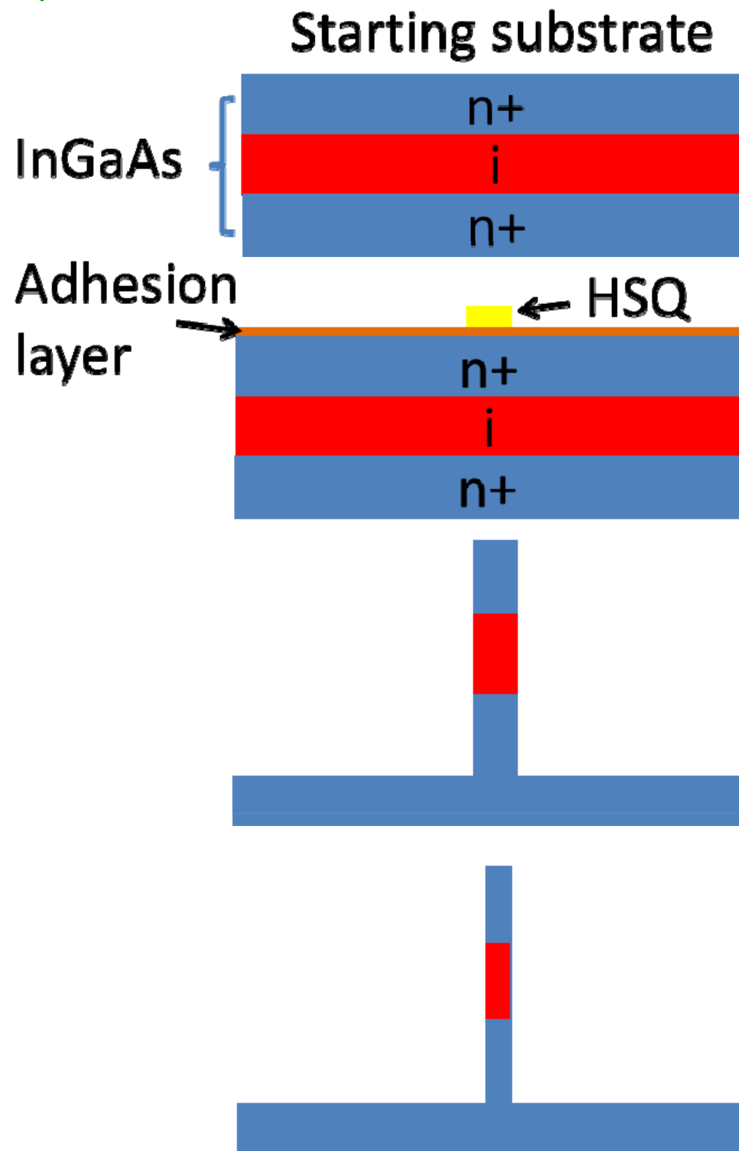
n+: 6×10^{19} cm^{-3} Si doping

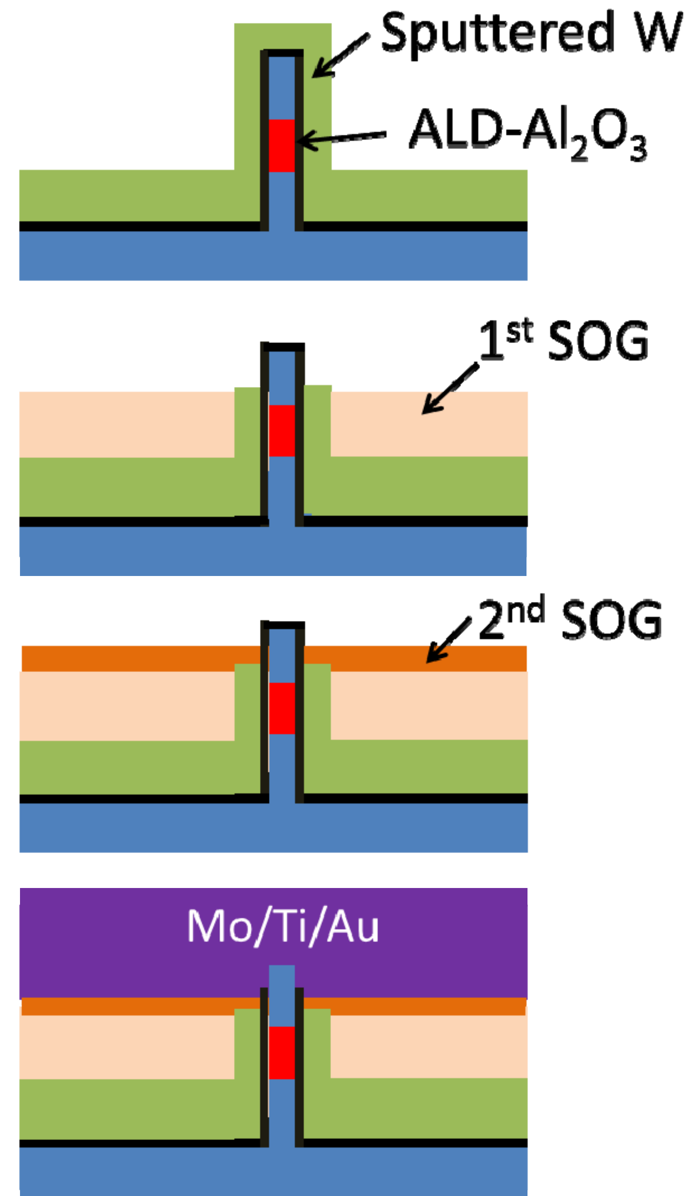


Top-down approach: flexible and manufacturable

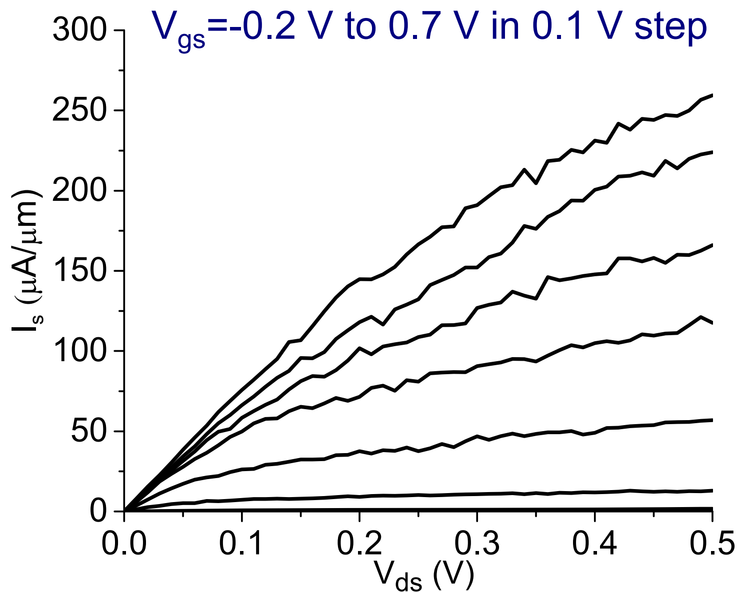
Tomioka, Nature 2012
Persson, DRC 2012
Zhao, IEDM 2013

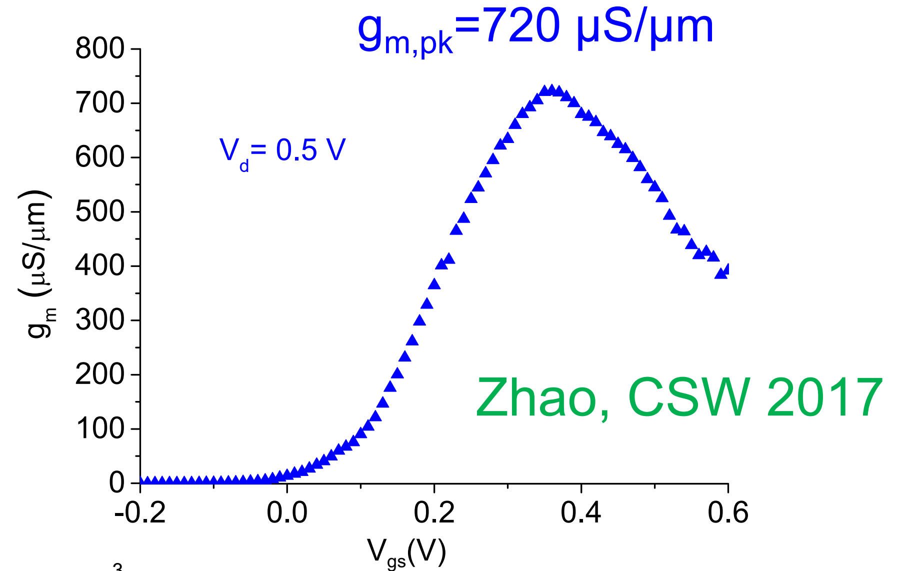
Process flow





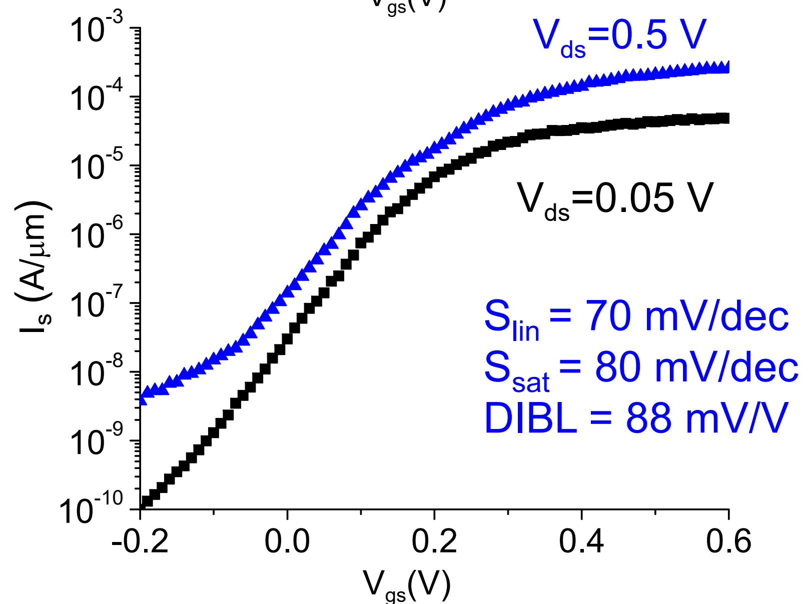
NW-MOSFET I-V characteristics: D=40 nm



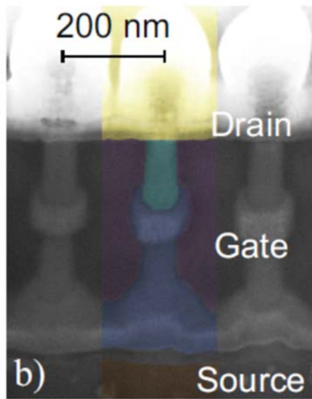


Single nanowire MOSFET:

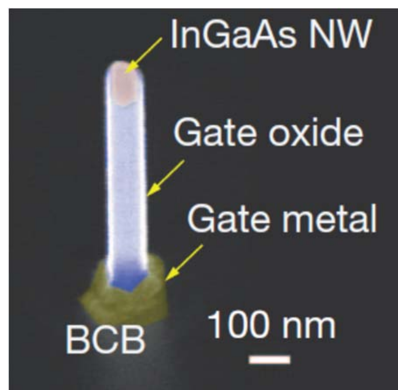
- L_{ch}= 80 nm
- 3 nm Al_2O_3 (EOT = 1.5 nm)
- $g_{m,pk}$=720 μS/μm @ V_{DS}=0.5 V
- S_{lin}=70 mV/dec, S_{sat}=80 mV/dec
- DIBL=88 mV/V



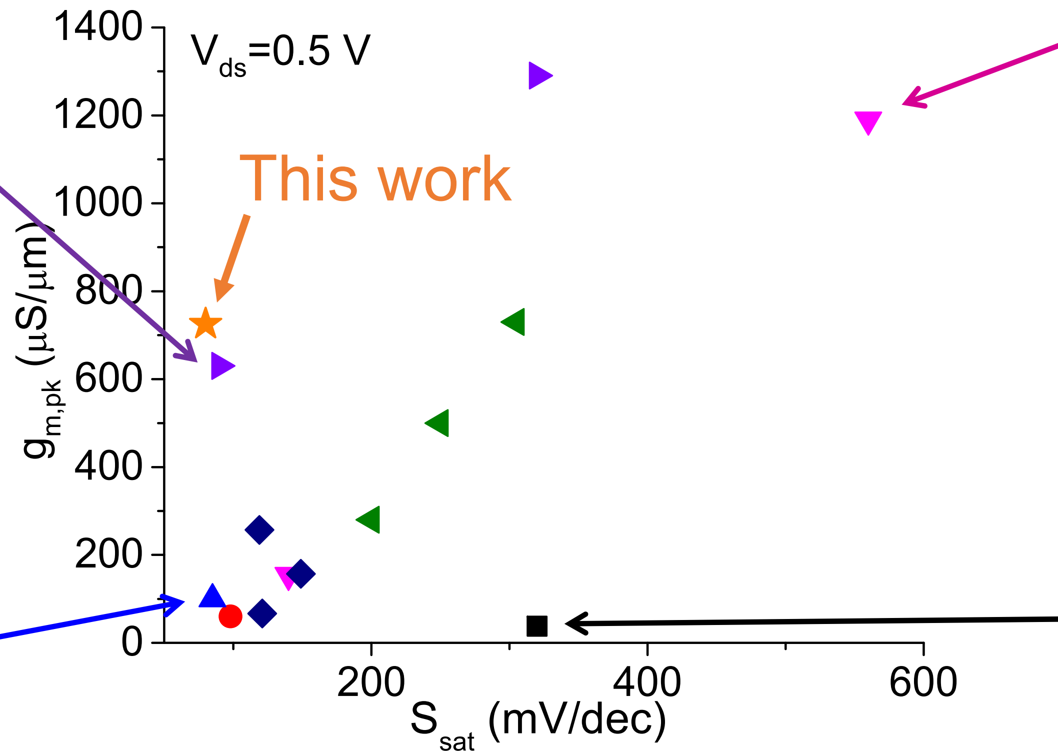
InGaAs VNW-MOSFETs Benchmark

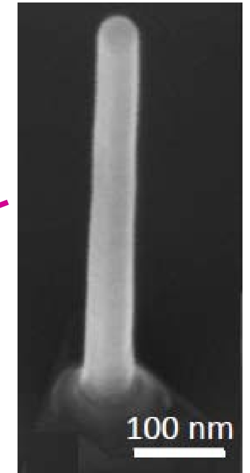


Berg, IEDM 2015

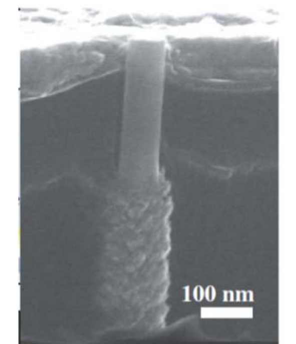


Tomioka, Nature 2012





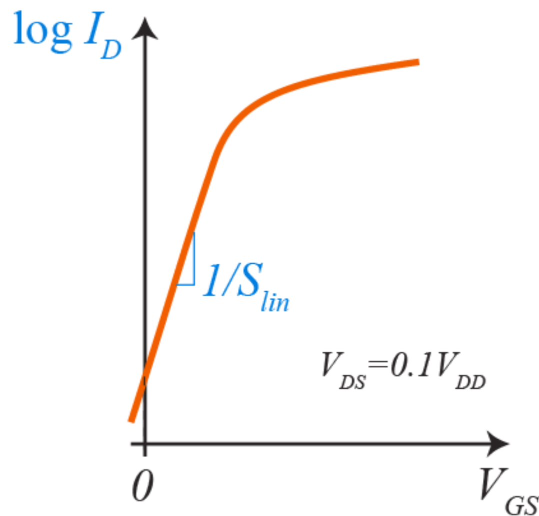
Persson, DRC 2012

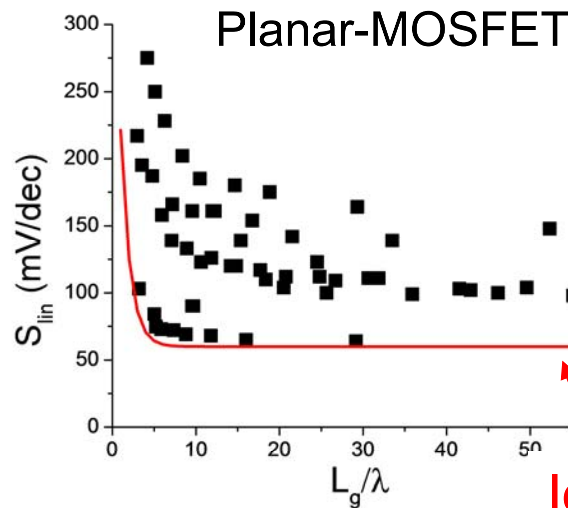


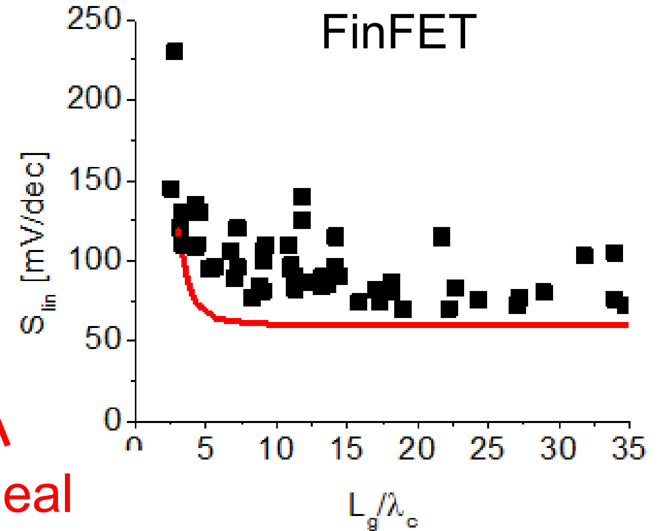
Tanaka, APEX 2010

Top-down VNW-MOSFETs as good as bottom up devices

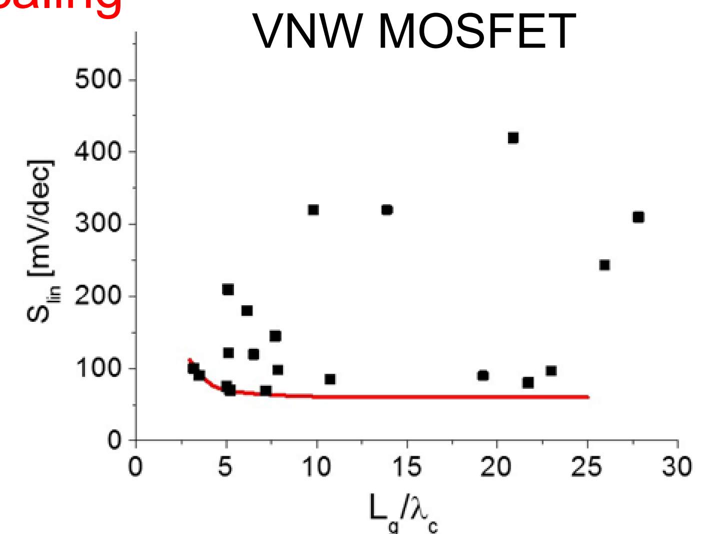
How are we doing in terms of short-channel effects?







Ideal scaling



S_{lin}: linear subthreshold swing

L_g= gate length

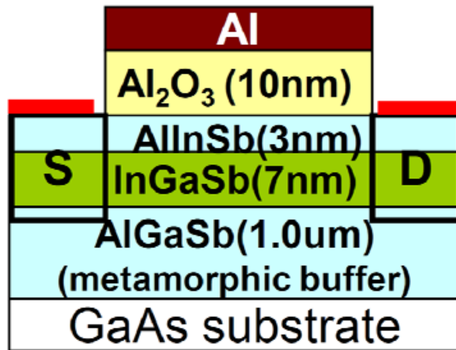
λ_c= electrostatic scaling length: f(t_{ox}, t_{ch})

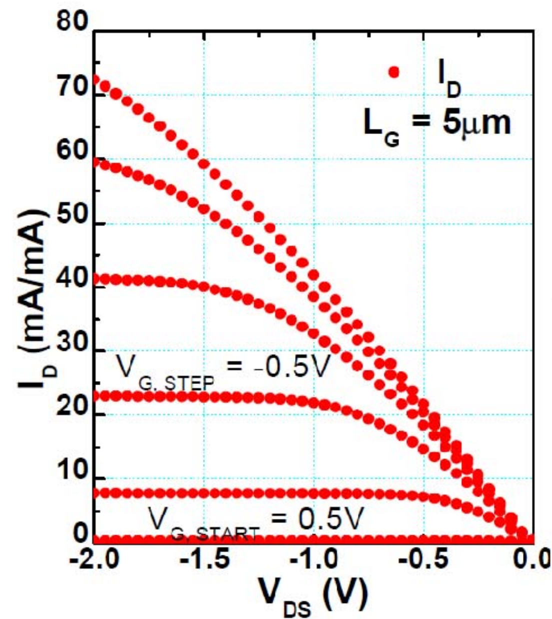
- Reasonable scaling behavior but…
- Excessive D_{it}

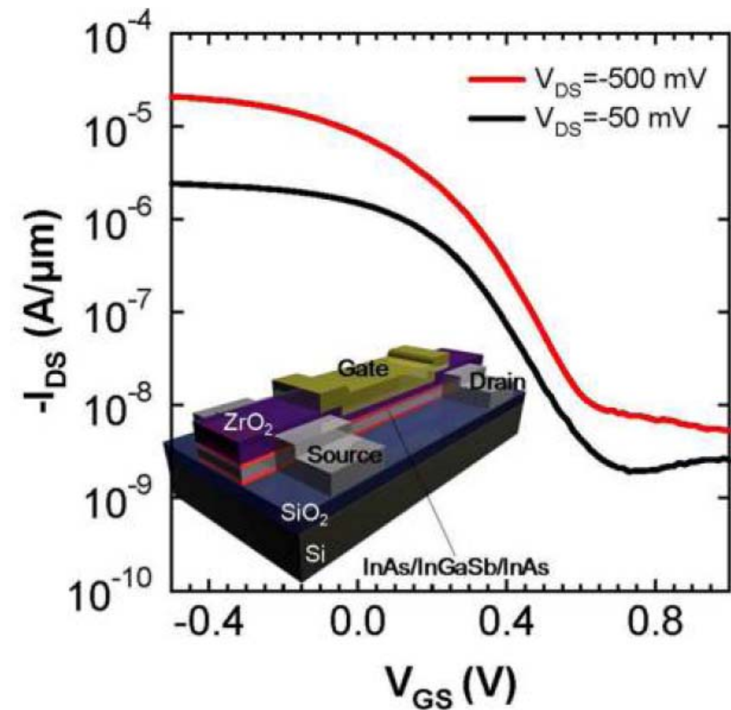
del Alamo, J-EDS 2016

4. InGaSb p–type MOSFETs

Planar InGaSb MOSFET demonstrations:







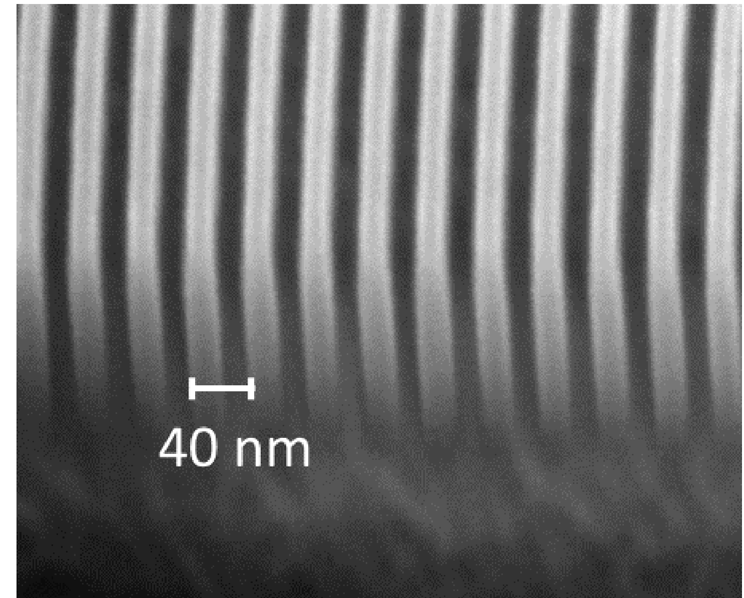
Nainani, IEDM 2010

Takei, Nano Lett. 2012

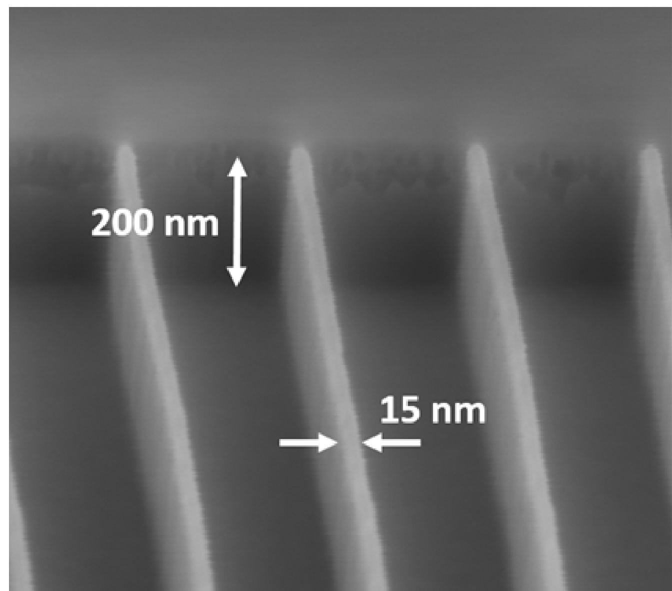
InGaSb p–type FinFETs @ MIT

Key enabling technology:

- BCl_3/N_2 RIE
- [digital etch under development]



20 nm fins, 20 nm spacing



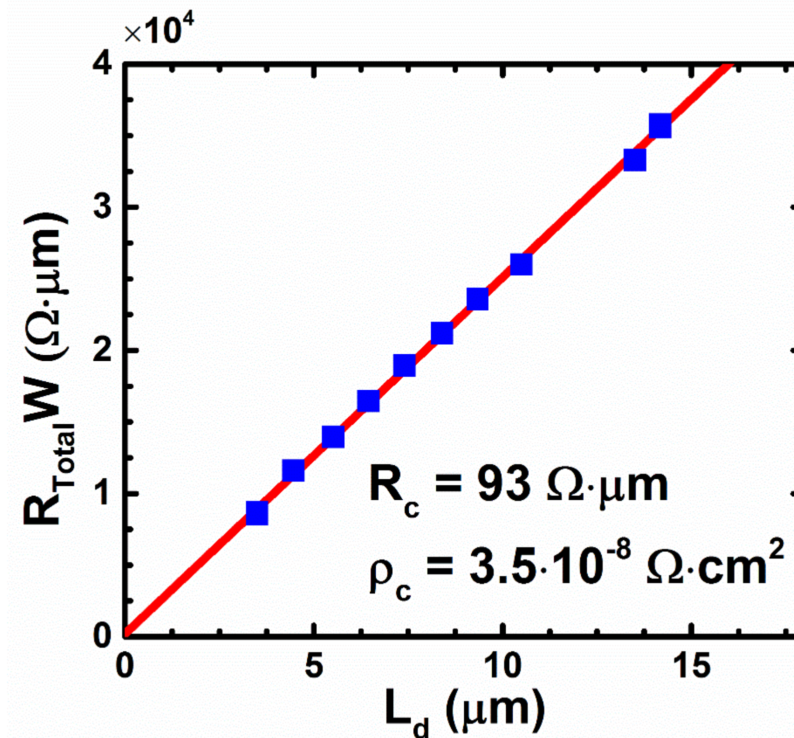
15 nm fins, AR>13

- Smallest W_f = 15 nm
- Aspect ratio >10
- Fin angle > 85°
- Dense fin patterns

Lu, IEDM 2015

Si-compatible contacts to p⁺-InAs

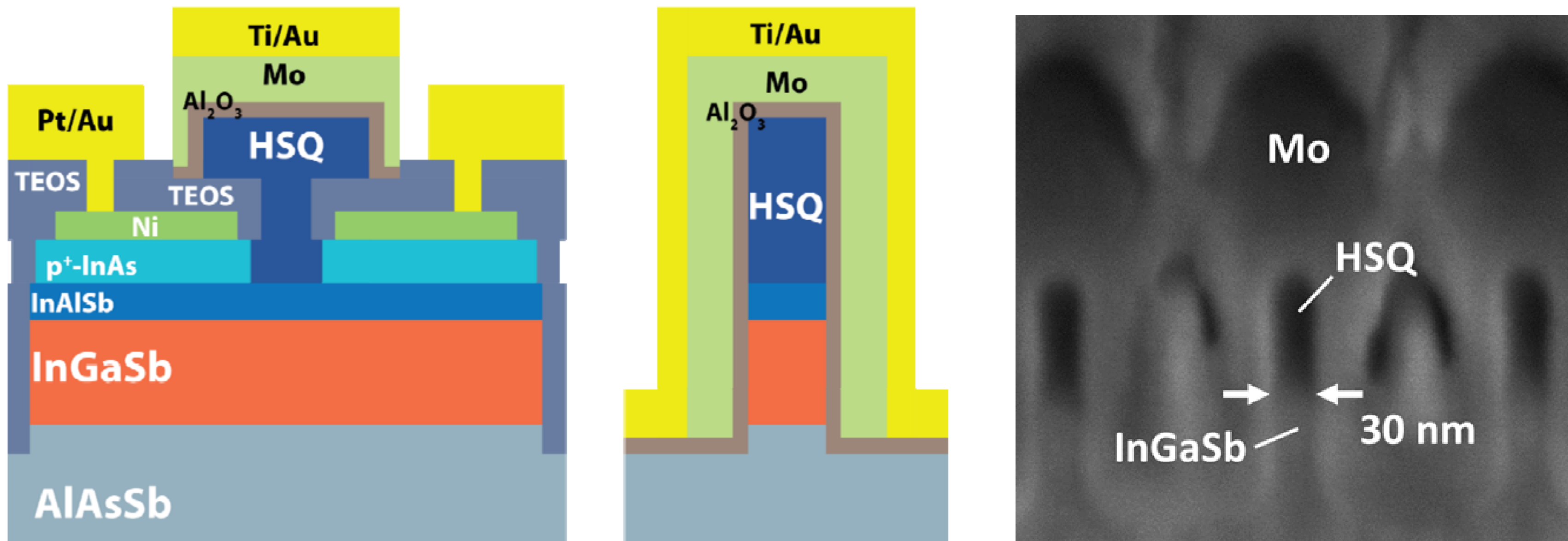
Ni/Ti/Pt/Al on p^+-InAs (circular TLMs):



Lu, IEDM 2015

Record ρ_c: 3.5×10^{-8} $\Omega.cm^2$ at 400^oC

InGaSb p-type FinFETs

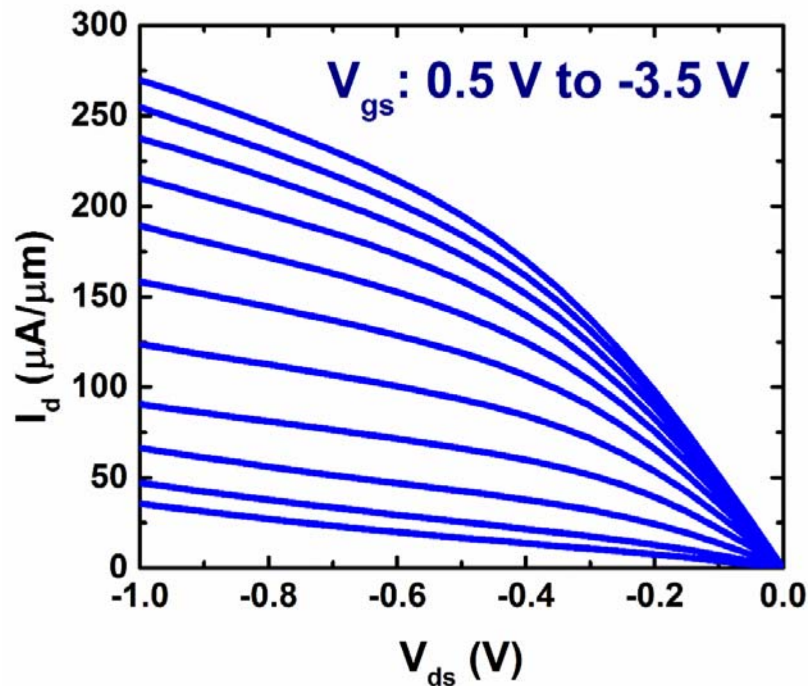


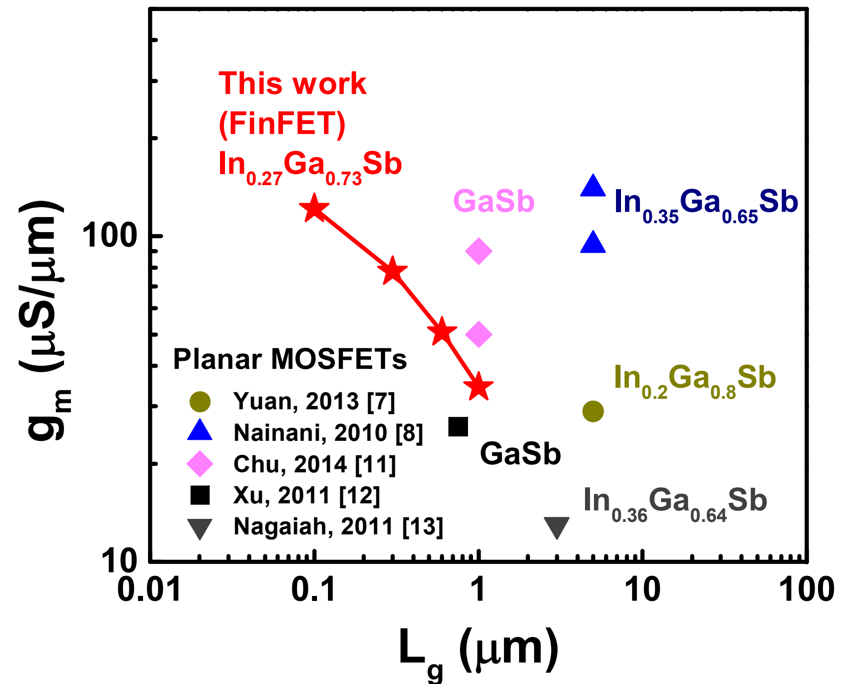
- Fin etch mask left in place → <u>double-gate MOSFET</u>
- Channel: 10 nm $In_{0.27}Ga_{0.73}Sb$ (compressively strained)
- Gate oxide: 4 nm Al_2O_3 (EOT=1.8 nm)

Lu, IEDM 2015

InGaSb FinFET I-V characteristics

- L_g = 100 nm, W_f = 30 nm (AR=0.33)
- Normalized by conducting gate periphery





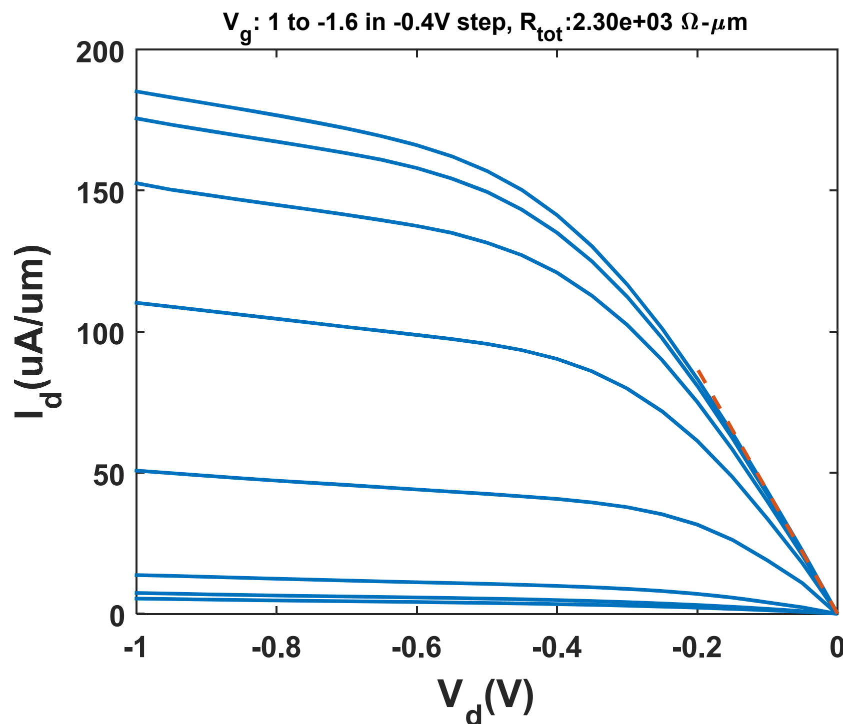
- First InGaSb FinFET
- Peak g_m approaches best InGaSb planar MOSFETs
- Poor turn off

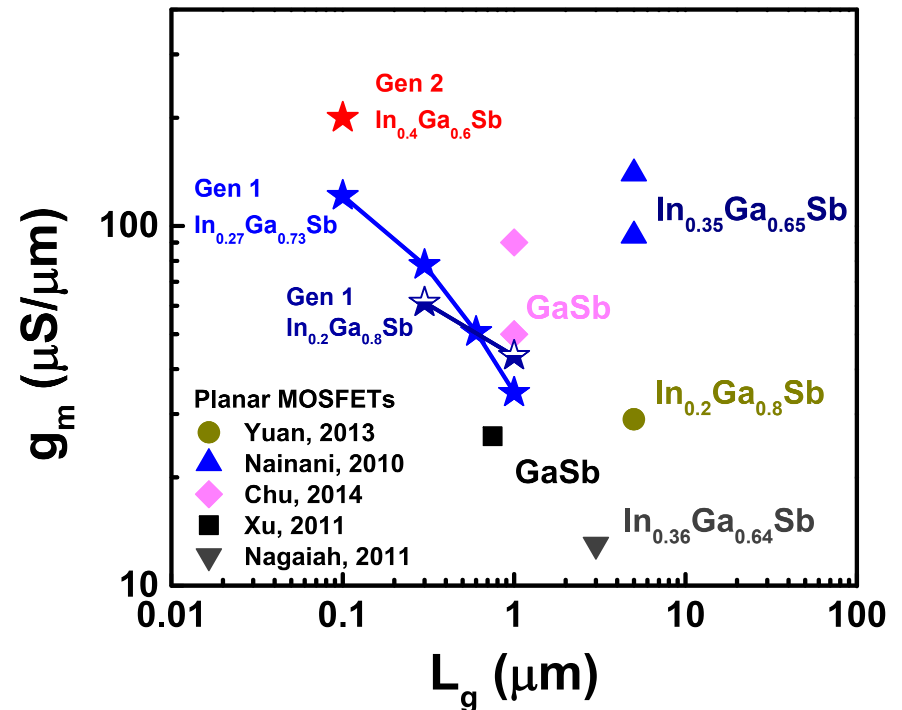
Lu, IEDM 2015

InGaSb p-Channel FinFETs (2nd gen.)

- L_g = 100 nm, W_f = 18 nm (AR=0.42)
- Channel: 7.5 nm $In_{0.4}Ga_{0.6}Sb$

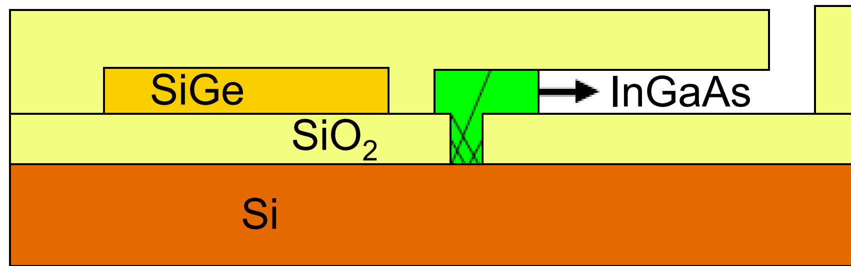
Lu, CSW 2017



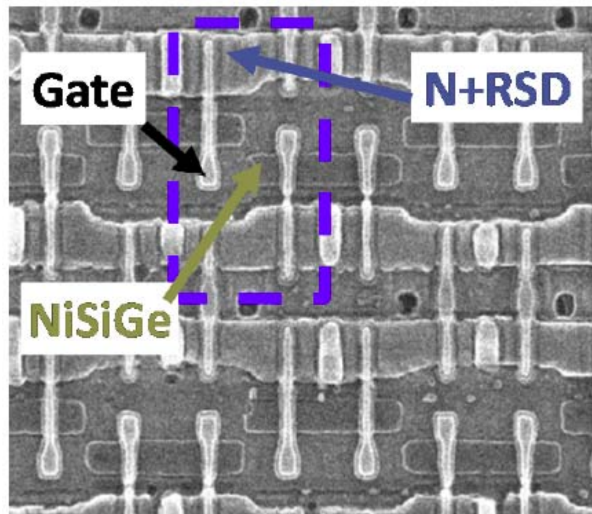


- $g_{m,max}$ = 200 μS/μm
- Still poor turn-off → need digital etch, better sidewall passivation

5. Co-integration of SiGe p-MOSFETs and InGaAs MOSFETs on SOI

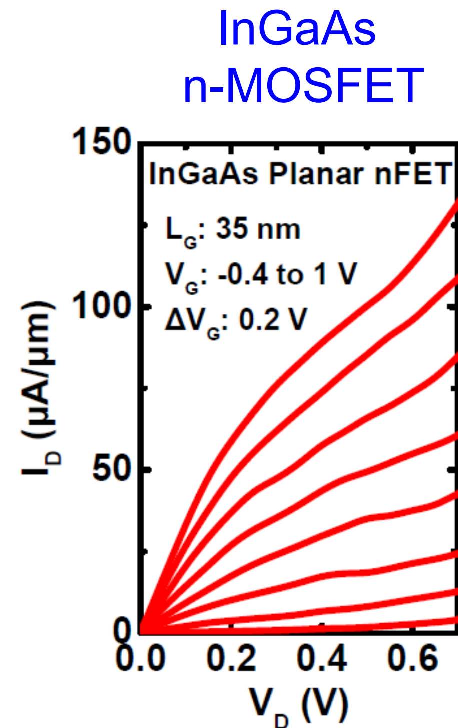


Confined Epitaxial Lateral Overgrowth

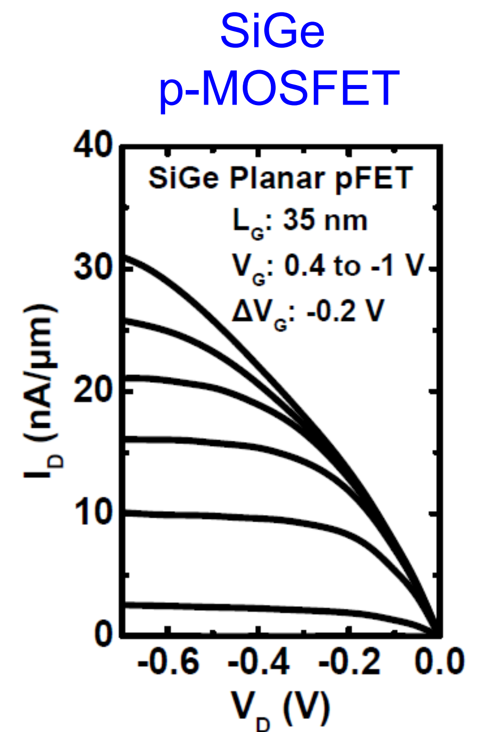


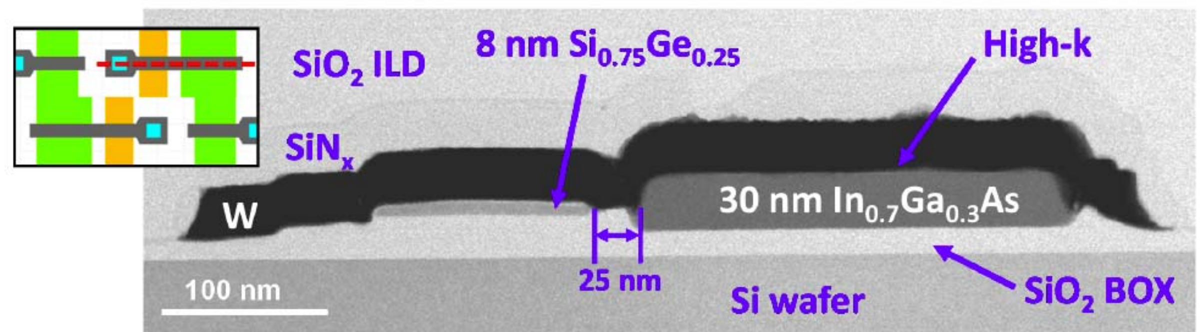
6T-SRAM

InGaAs n-MOSFET



SiGe p-MOSFET





Czornomaz, VLSI Tech 2016

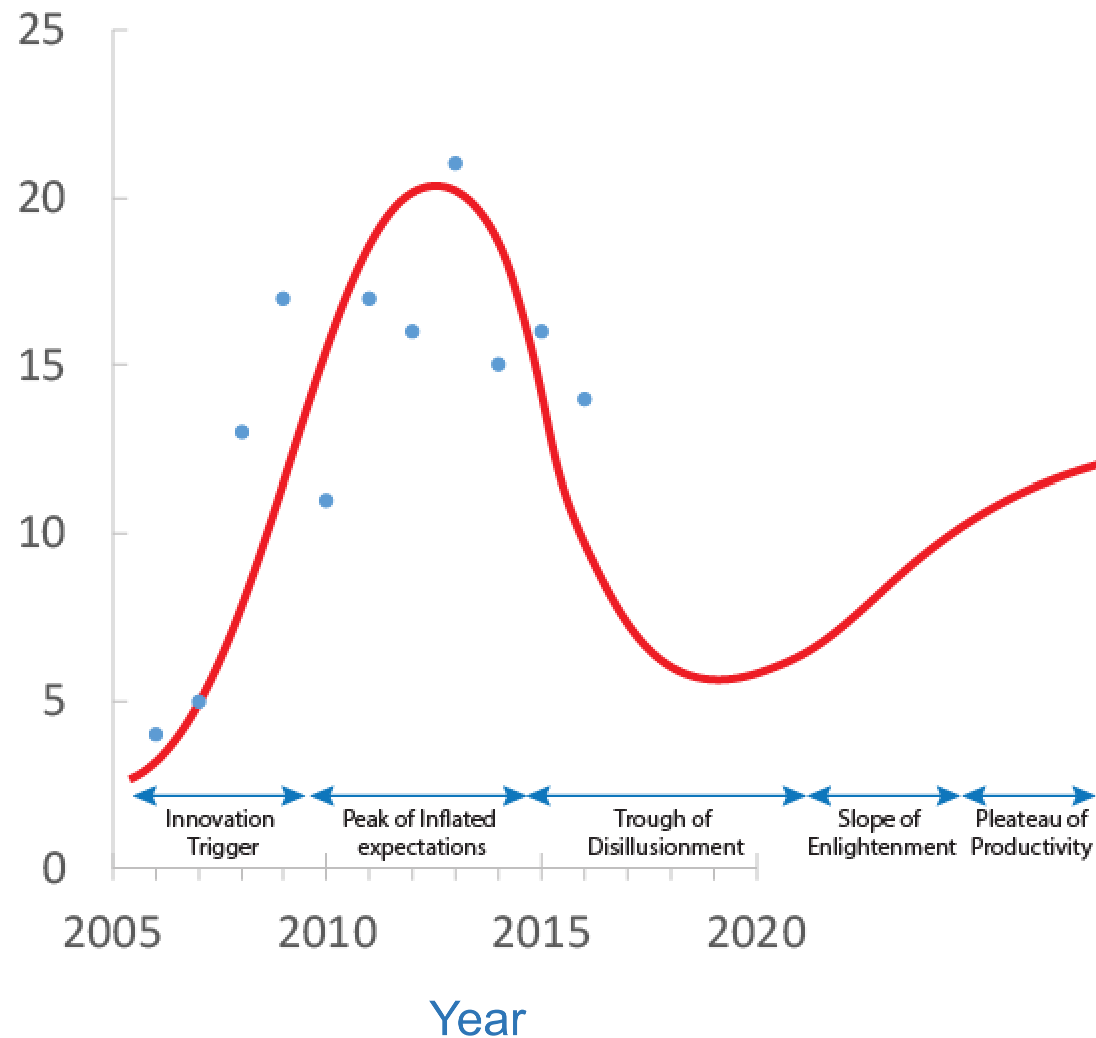
Conclusions

1. Great recent progress on planar, fin and nanowire InGaAs MOSFETs
2. Device performance still lacking for multigate designs
3. P-type InGaSb MOSFETs in their infancy
4. Many, MANY issues to work out:

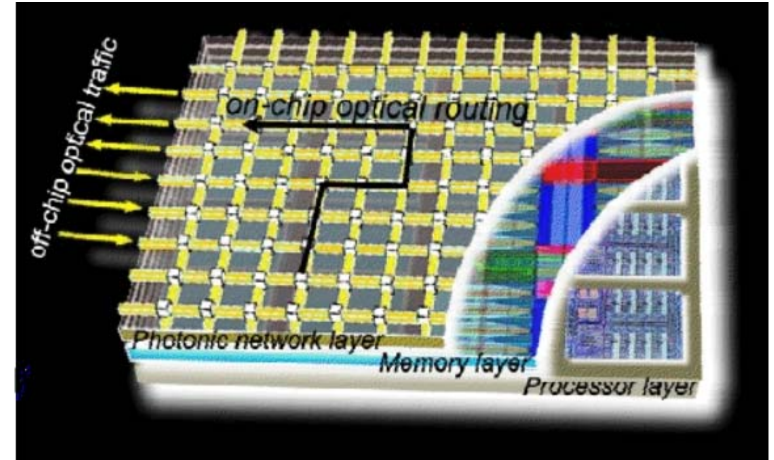
sub-10 nm fin/nanowire fabrication, self-aligned contacts, device asymmetry, introduction of mechanical stress, V_T control, sidewall roughness, device variability, BTBT and parasitic HBT gain, trapping, self-heating, reliability, NW survivability, co-integration on n- and p-channel devices on Si, …

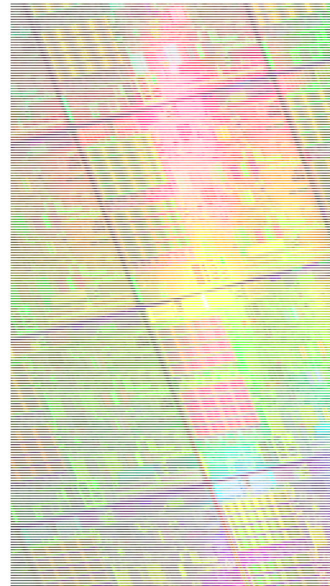
Hype curve for III-V CMOS?

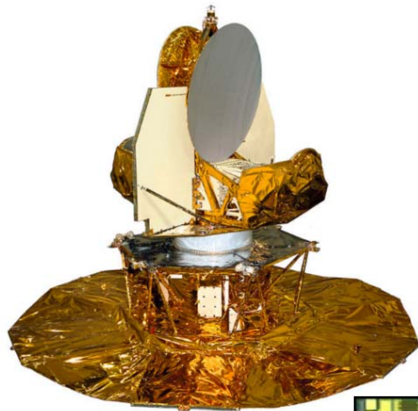
\# Papers on
III-V CMOS
at IEDM

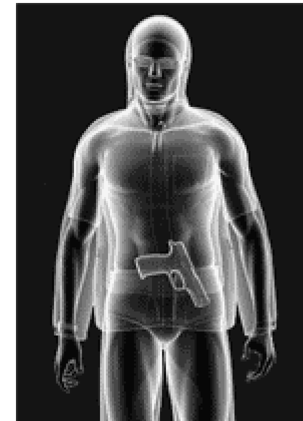


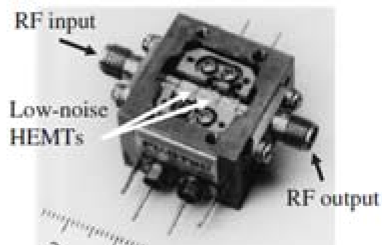
A lot of work ahead but...
exciting future for III-V electronics

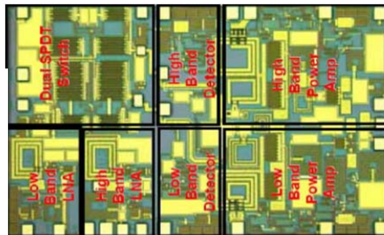












INTEGRATED MICROELECTRONIC DEVICES

J. A. del Alamo